

Timing Analysis of Software Executing on Undocumented Multicore Processors

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Carnegie Mellon University

Software Engineering Institute

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Systems Interact with Their Physical Environment



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Systems Include Software



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Systems Include Software That Interacts with the Physical Environment



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Systems Include Software That Has Real-Time Requirements



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Satisfying Real-Time Requirements is a Challenge for These Systems in General



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"The trick there, when you're processing flight critical information, it has to be a deterministic environment, meaning we know exactly where a piece of data is going to be exactly when we need to — no room for error," Langhout says. "On a multi-core processor there's a lot of sharing going on across the cores, so right now we're not able to do that." - Jeff Langhout, Acting Director, U.S. Army Aviation and Missile Research Development and Engineering Center (AMRDEC)

Source: "Army still working on multi-core processor for UH-60V," May 2017, Available at https://www.flightglobal.com/news/articles/army-still-working-on-multi-core-processor-for-uh-6-436895/.

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"A majority of avionics today are running on single-core processors, or multicore processors with all but one core disabled."

"The root of the problem is shared resources, which most of the time creates some kind of interference."

Source: "It's time: Avionics need to move to multicore processors," January 2018, Available at http://www.intelligent-aerospace.com/articles/2018/01/it-s-time-avionics-needs-to-move-to-multicore-processors.html.

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"In safety-critical domains such as avionics, the multicore "predictability problem" is currently dealt with by turning off all but one core if highly-critical system components exist."

Source: C. J. Kenna et al., "Making Shared Caches More Predictable on Multicore Platforms," RTSS'2012.

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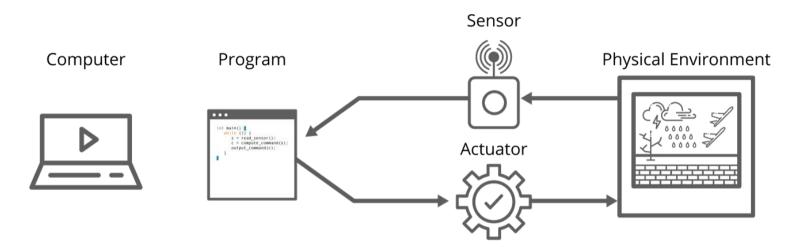
"Currently, avionics manufacturers resolve the multicore "predictability problem" by turning off all but one core if highly critical system components exist."

Source: B. C. Ward et al., "Making Shared Caches More Predictable on Multicore Platforms," ECRTS'2013.

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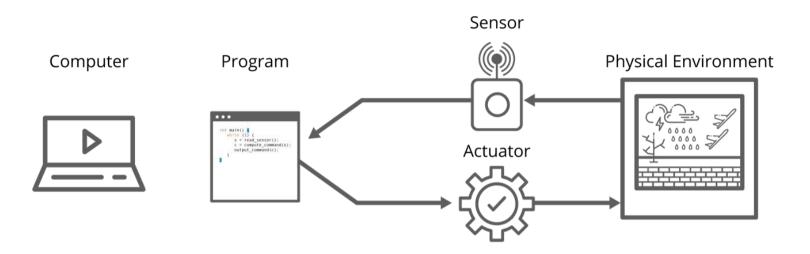
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Commonality of these Systems



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Commonality of these Systems

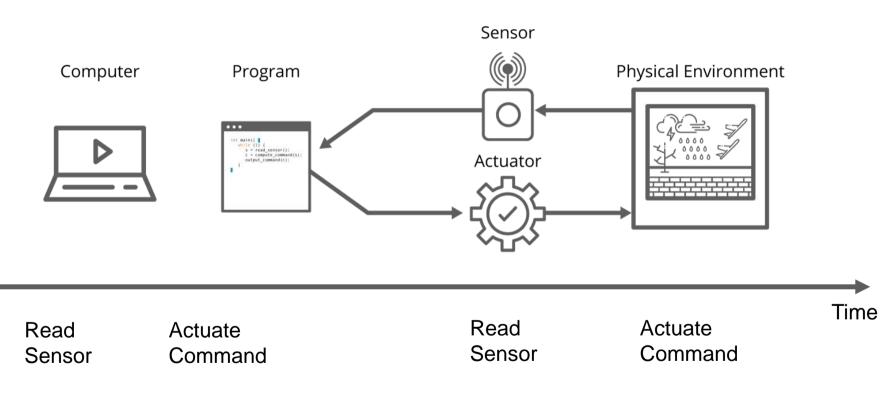


	Time
Actuate	
Commanu	
	Actuate Command

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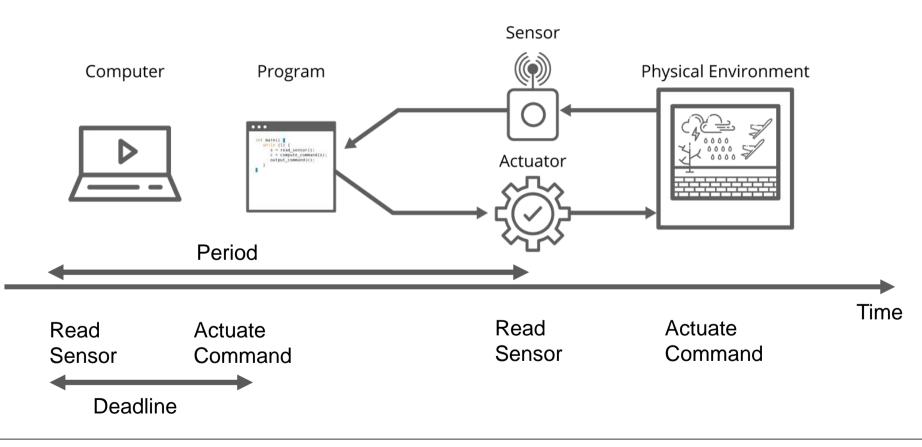
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Commonality of these Systems



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Commonality of these Systems

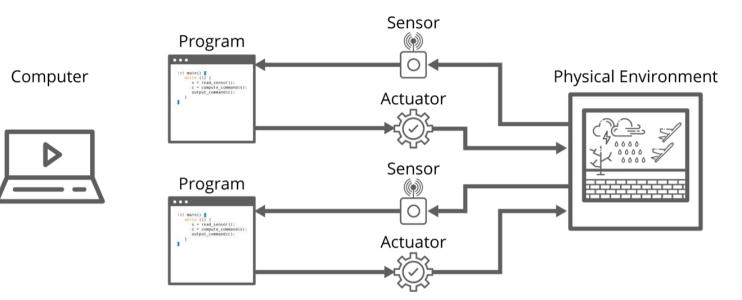


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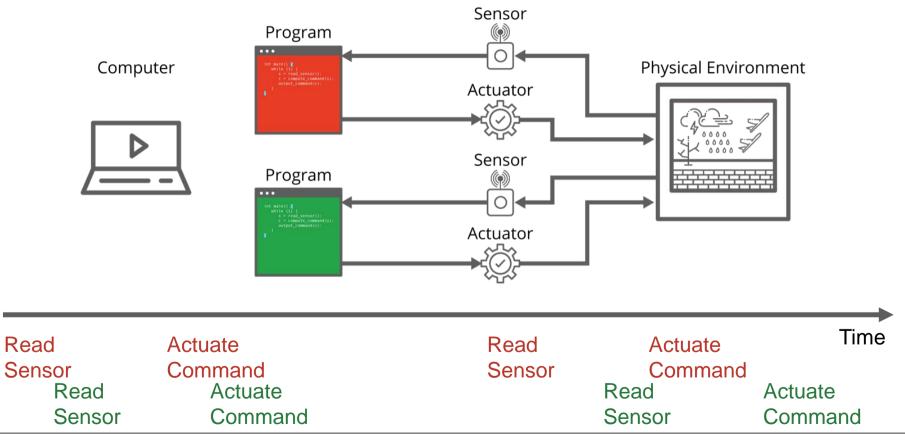
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Commonality of these Systems



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Commonality of these Systems



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What Makes it Challenging to Satisfy Real-Time Requirements?

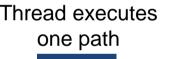


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Time when one thread in the software system arrives

Deadline Time

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Time when one thread in the software system arrives

Deadline Time

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Thread executes another path

Time when one thread in the software system arrives

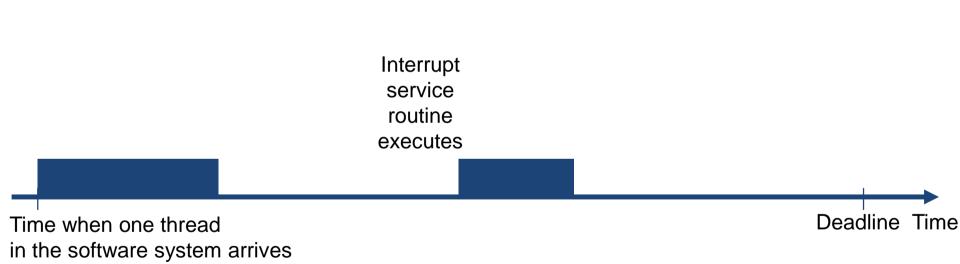
Deadline Time

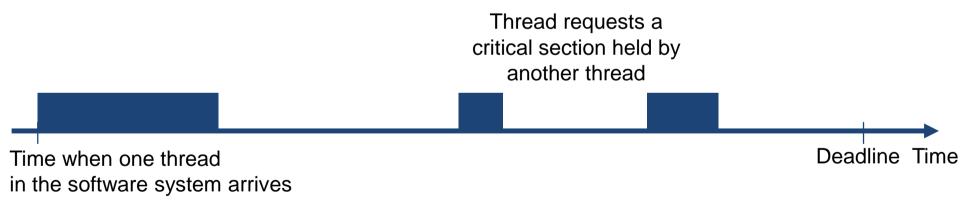
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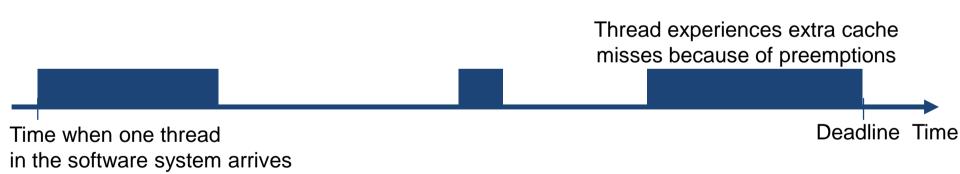
Preemption: Another thread uses the processor.

Time when one thread in the software system arrives

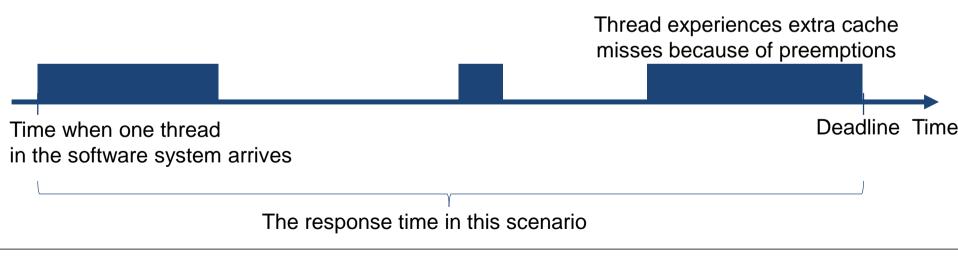
Deadline Time





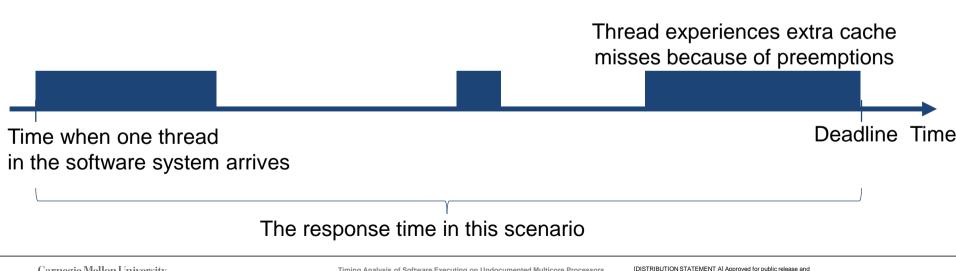


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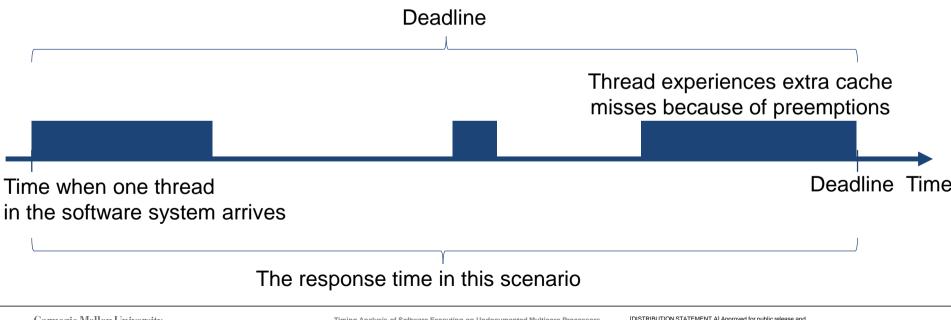
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How large can the response time be?



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Does it hold for all scenarios that the response time is at most the deadline?



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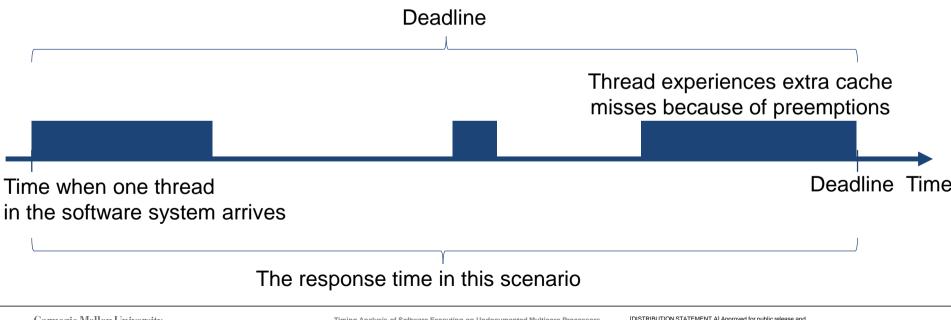
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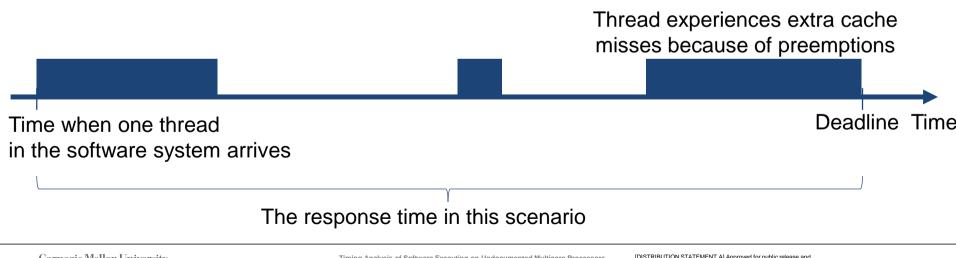
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Does it hold for all scenarios that the response time is at most the deadline?



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Does it hold for all threads, that for all arrivals of the thread, that for all scenarios, that the finishing time is at most the deadline?



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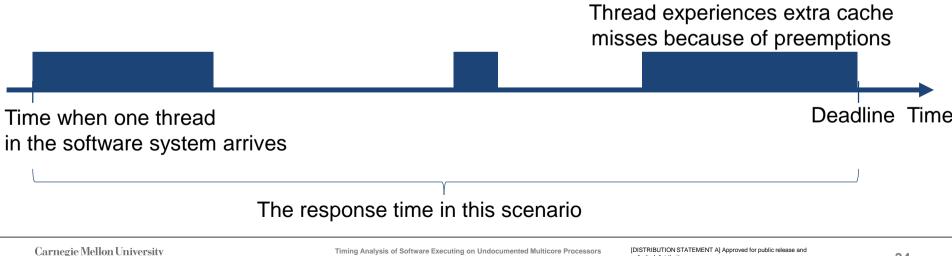
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What Causes Delay of Software?

Does it hold for all threads. that for all arrivals of the thread. that for all scenarios. that the finishing time is at most the deadline?

If "yes," we say the set of threads is *schedulable*. Otherwise, the set of threads is unschedulable.



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What Causes Delay of Software?

Does it hold for all threads, that for all arrivals of the thread, that for all scenarios, that the finishing time is at most the deadline?

If "yes," we say the set of threads is *schedulable*. Otherwise, the set of threads is *unschedulable*.

The process of determining whether a set of threads is schedulable is called *schedulability analysis*.

Thread experiences extra cache misses because of preemptions

Time when one thread in the software system arrives

The response time in this scenario

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Time

Deadline

Conclusions so far

Many systems interact with the physical world

This interaction requires correct timing

Correct timing depends on the whether the delay of the software is at most a certain bound

There are many causes of the delay of software (even on a computer with a single core)

Many systems today disable all processor cores except one in order to be confident about timing

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Real-Time Requirements of Software Executing on a Multicore Processor

Hardware Trends

• All computers are multicores.

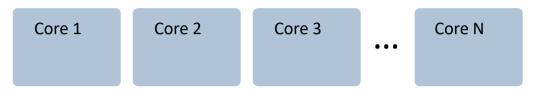


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Real-Time Requirements of Software Executing on a Multicore Processor

Hardware Trends

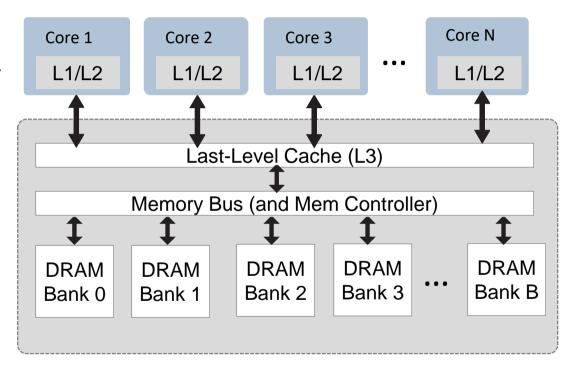
- All computers are multicores.
- Most chip makers do not offer single core.



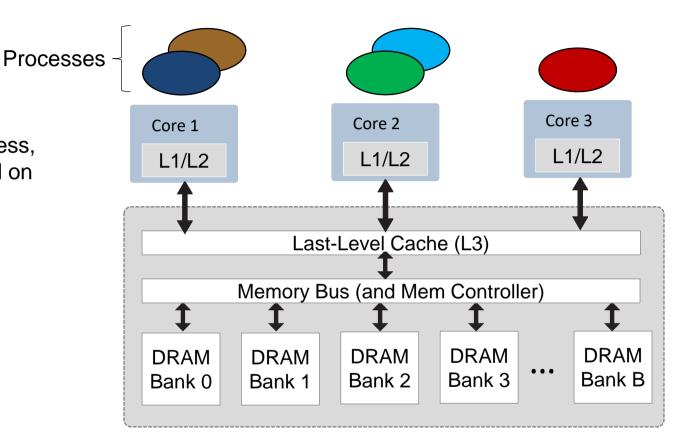
Real-Time Requirements of Software Executing on a Multicore Processor

Hardware Trends

- All computers are multicores.
- Most chip makers do not offer single core.
- Most multicores have shared memory.

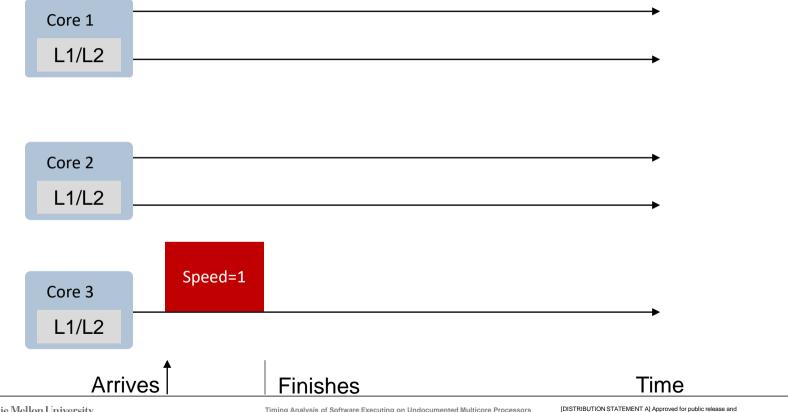


Problem: For each process, compute an upper bound on its response time.



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How Co-Runners Impact Speed of Execution

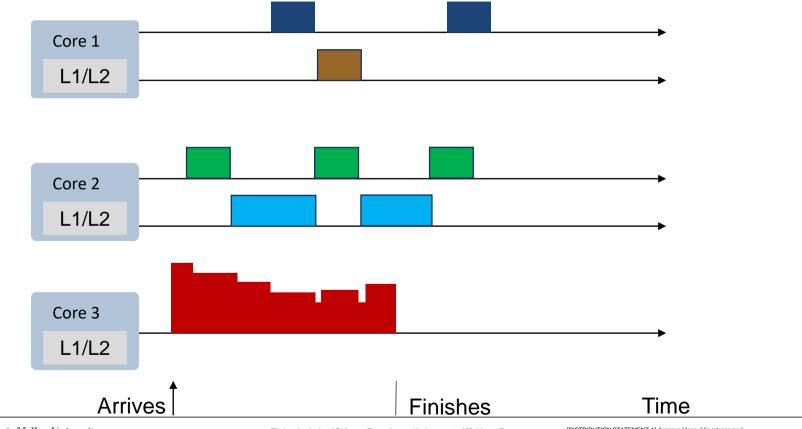


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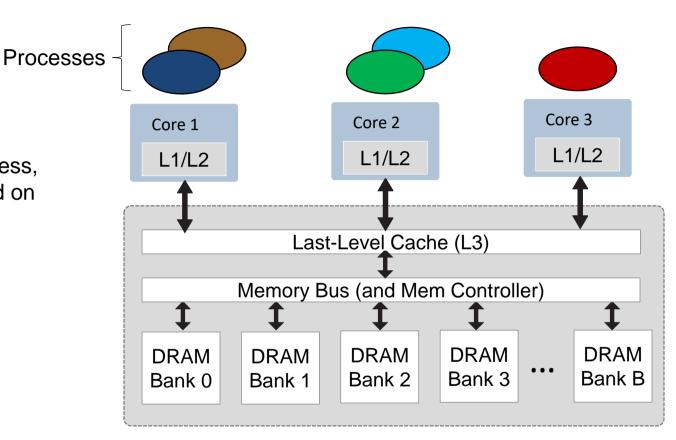
How Co-Runners Impact Speed of Execution



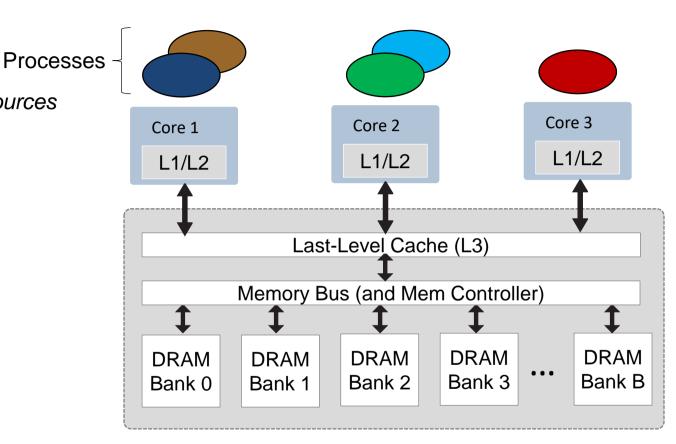
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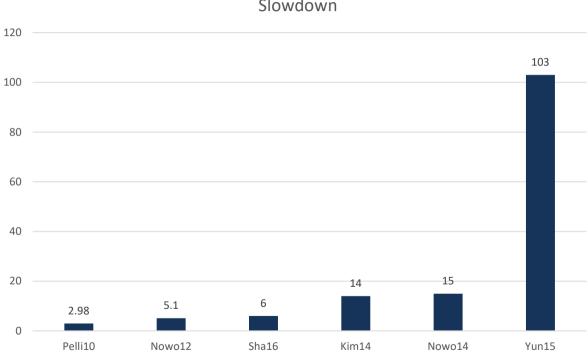
• Shared hardware resources impact timing.



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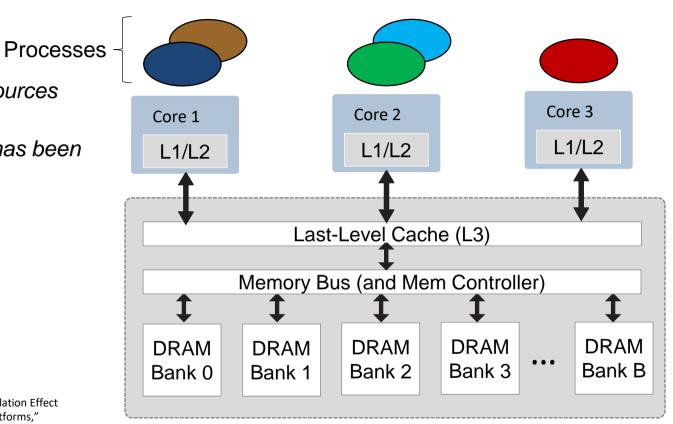
Slowdown

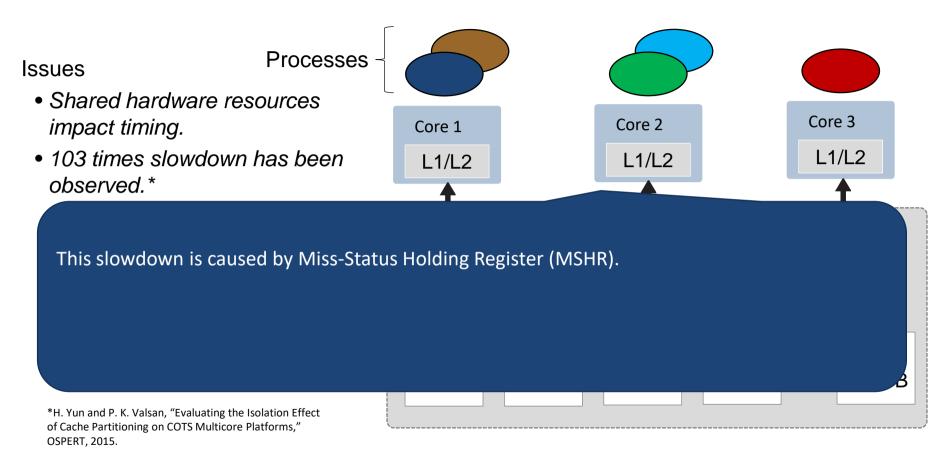
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- Shared hardware resources impact timing.
- 103 times slowdown has been observed.*

*H. Yun and P. K. Valsan, "Evaluating the Isolation Effect of Cache Partitioning on COTS Multicore Platforms," OSPERT, 2015.





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- Shared hardware resources impact timing.
- 103 times slowdown has been observed.*

This slowdown is caused by Miss-Status Holding Register (MSHR). At that time, most researchers in real-time systems community were not aware of the MSHR.

Core 1

L1/L2

Processes

*H. Yun and P. K. Valsan, "Evaluating the Isolation Effect of Cache Partitioning on COTS Multicore Platforms," OSPERT, 2015. Core 2

L1/L2

Core 3

L1/L2

- Shared hardware resources impact timing.
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Processes

This slowdown is caused by Miss-Status Holding Register (MSHR). At that time, most researchers in real-time systems community were not aware of the MSHR. There was no schedulability analysis that incorporated MSHR.

Core 1

L1/L2

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L1/L2

Core 3

L1/L2

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Processes

This slowdown is caused by Miss-Status Holding Register (MSHR). At that time, most researchers in real-time systems community were not aware of the MSHR. There was no schedulability analysis that incorporated MSHR. Even today, there is no schedulability analysis that incorporated MSHR.

Core 1

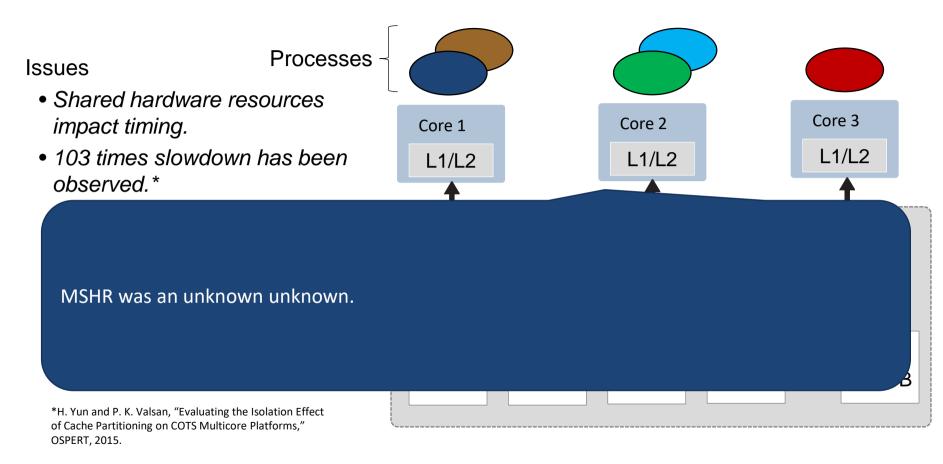
L1/L2

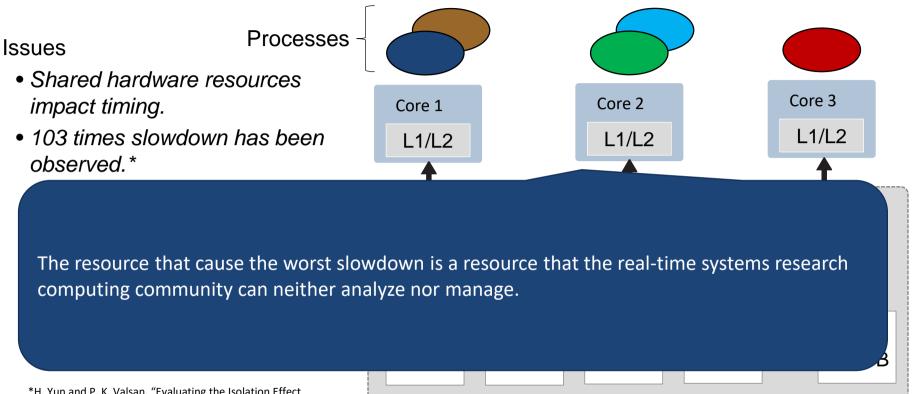
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L1/L2

Core 3

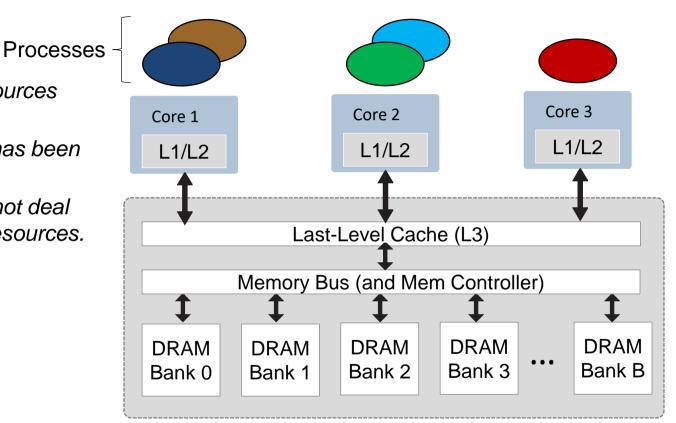
L1/L2



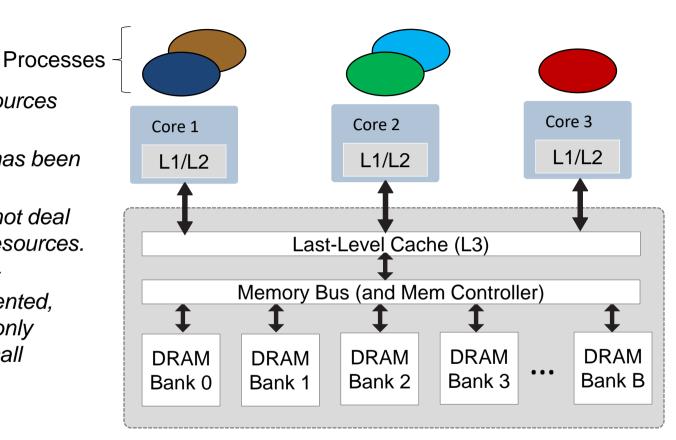


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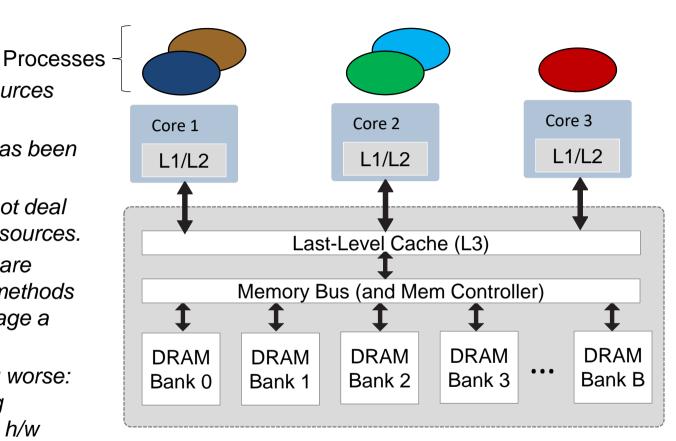
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- 103 times slowdown has been observed [Yun15].
- Current methods cannot deal with undocumented resources.



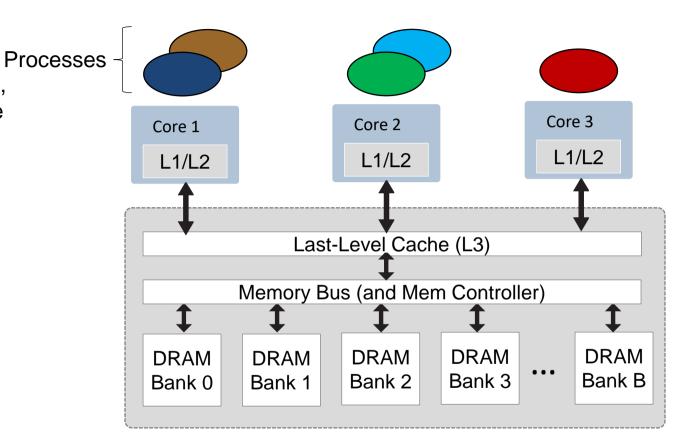
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- Even for the case that resources are documented, current methods can only analyze/manage a small set of them.



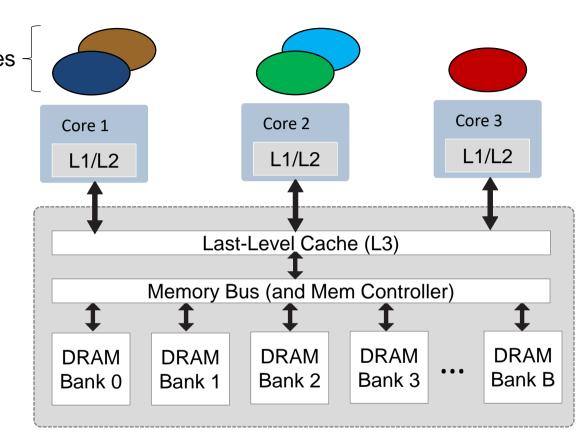
- Shared hardware resources impact timing.
- 103 times slowdown has been observed [Yun15].
- Current methods cannot deal with undocumented resources.
- Even when resources are documented, current methods can only analyze/manage a small set of them.
- The problem is getting worse:
 - * Slowdown increasing
 - * More undocumented h/w



Problem: For each process, compute its response time



Processes - **Problem:** For each process, compute an upper bound on its response time

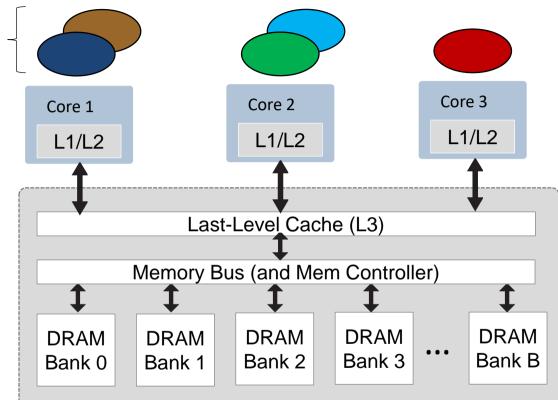


Processes -

Problem: For each process, compute an upper bound on its response time considering contention for resources in the memory system

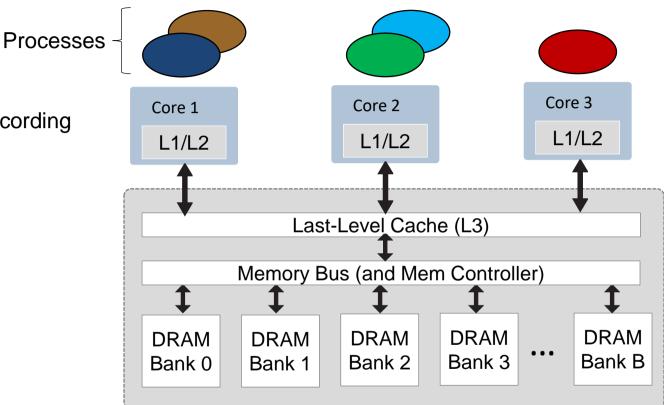
and

that resources in the memory system are undocumented.



Documented resources

 DRAM memory timing tends to be specified according to JDEC standard.

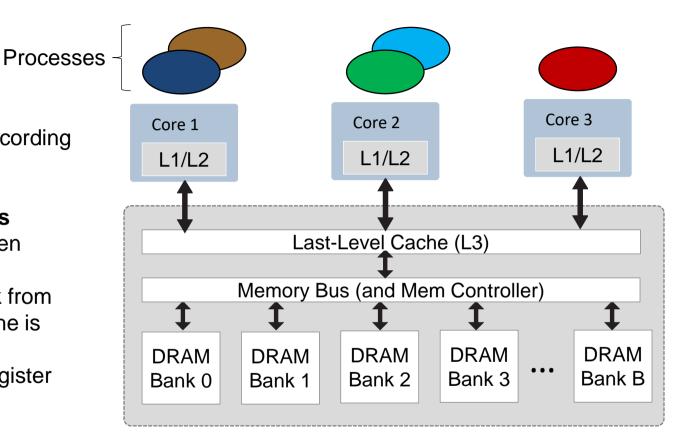


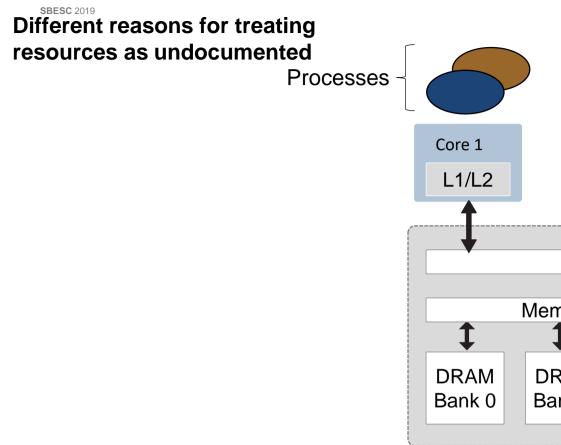
Documented resources

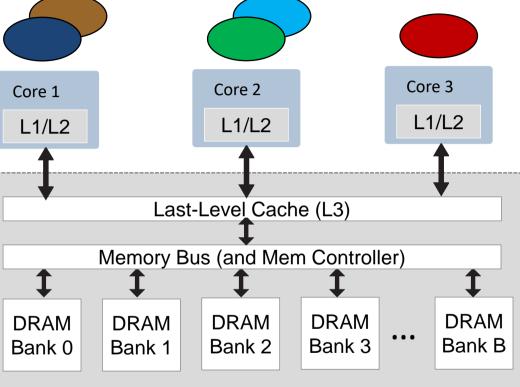
 DRAM memory timing tends to be specified according to JDEC standard.

Undocumented resources

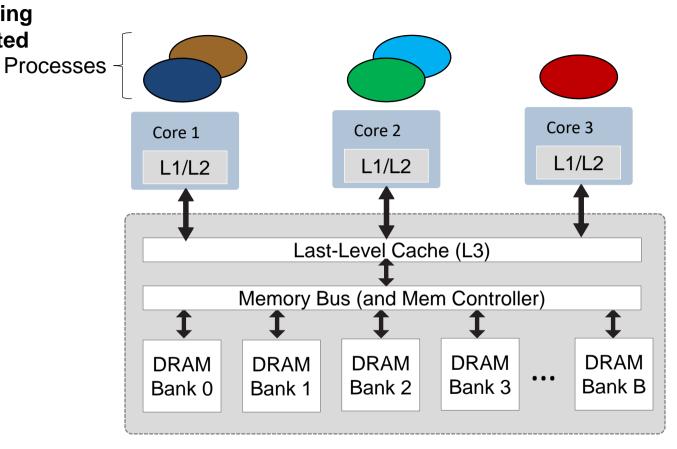
- Memory controller is often undocumented.
- Interconnection network from cores to Last-Level cache is often undocumented.
- Miss-Status Holding Register is often undocumented.



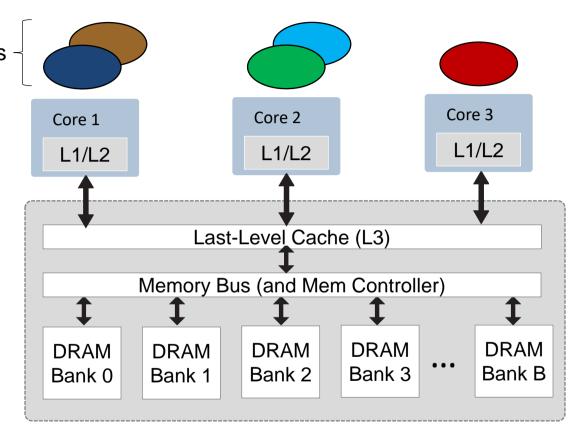




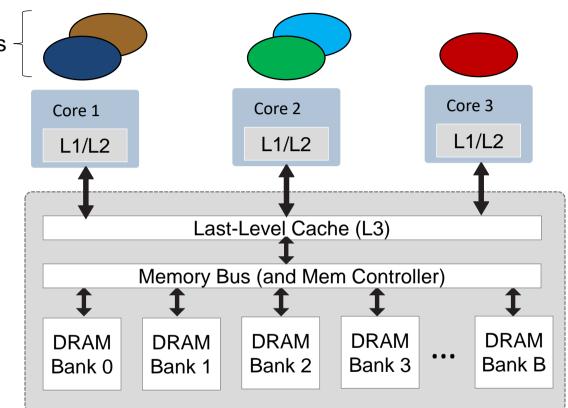
 Resources are undocumented



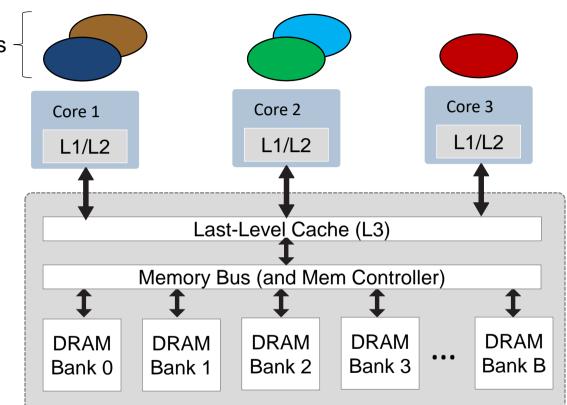
- Resources are Processes undocumented
- Resources are documented but documentation is incorrect



- Resources are Processes undocumented
- Resources are documented but documentation is incorrect
 - Heule:PLDI16:
 50 out of 1795 x86
 instructions have incorrect
 documentation

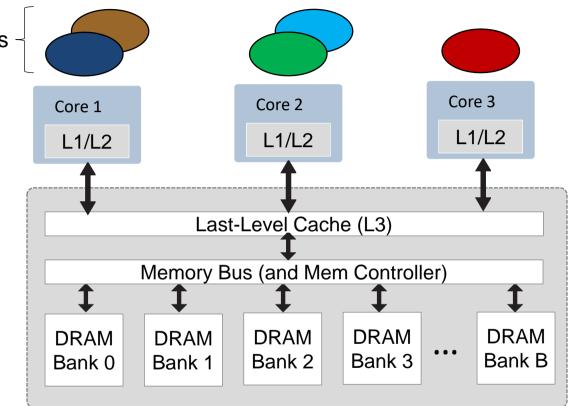


- Resources are Processes undocumented
- Resources are documented but documentation is incorrect
 - Heule:PLDI16: 50 out of 1795 x86 instructions have incorrect documentation
 - Dasgupta:PLDI19: Found incorrect documentation of instructions for x86.

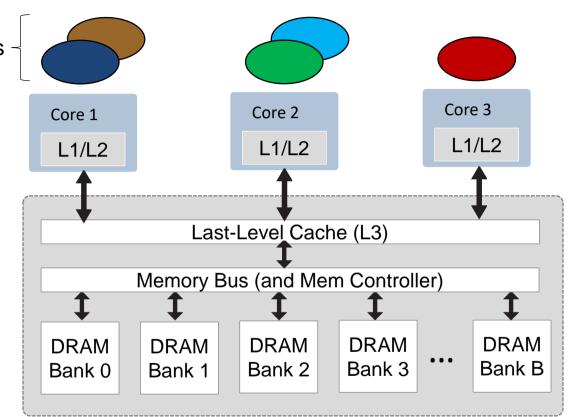


- Resources are Processes undocumented
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 - Fog19:

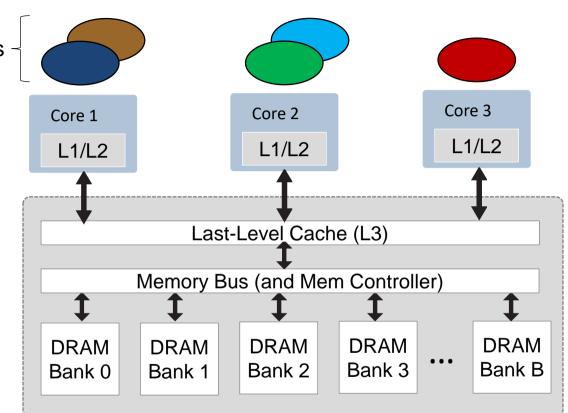
There are discrepancies between measured latencies and latencies in data sheets.



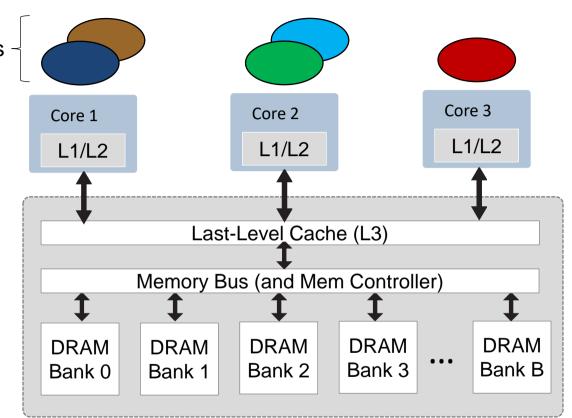
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- Resources are documented but one believes the documentation to be incorrect



- Resources are Processes undocumented
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- Resources are documented but one believes the documentation to be incorrect
- Resources are documented and one believe documentation to be correct but it is laborious to create a timing model for schedulability analysis



- Resources are Processes
 undocumented
- Resources are documented but documentation is incorrect
- Resources are documented but one believes the documentation to be incorrect
- Resources are documented and one believe documentation to be correct but it is laborious to create a timing model for schedulability analysis (and it needs to be changed when one buys a new chip anyway)



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The consequences of analyzing timing of software executing on multicores using documentation

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The consequences of analyzing timing of software executing on multicores using documentation

time

The consequences of analyzing timing of software executing on multicores using documentation

time

Project
starts:
We
want
to
develop
product
Х

time

Project	Buy
starts:	multi-

We core

want proc-

to essor

develop Y

product

Х

time

Project starts: We	Buy multi- core	Read data sheets
want to	proc-	of multicore
	essor	
develop	Y	processor
product		Y
Х		

time

Project	Buy	Read	Create
starts:	multi-	data	model of
We	core	sheets	hardware and
want	proc-	of	develop
to	essor	multicore	schedulability
develop	Y	processor	analysis
product		Υ	equations
Х			

time

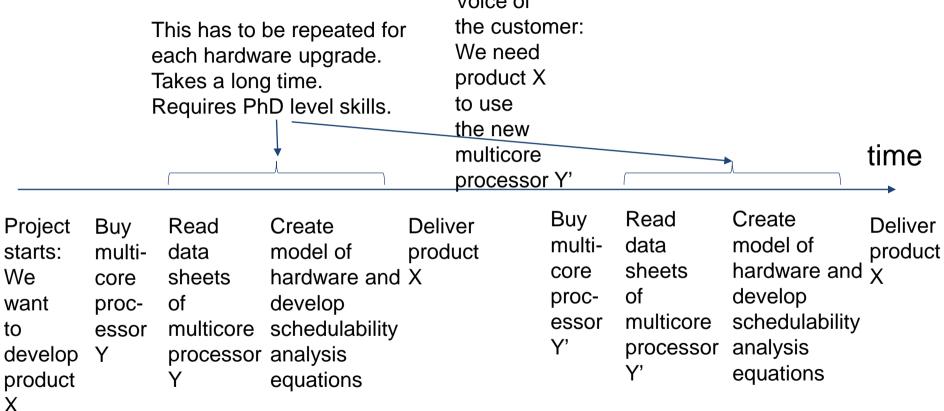
Project	Buy	Read	Create	Deliver
starts:	multi-	data	model of	product
We	core	sheets	hardware and	Х
want	proc-	of	develop	
to	essor	multicore	schedulability	
develop	Y	processor	analysis	
product		Υ	equations	
Х				

The consequences of analyzing timing of software executing on multicores using documentation Voice of the customer: We need product X to use the new multicore processor Y'

Project starts: We want	Buy multi- core proc-	Read data sheets of	Create model of hardware and develop	Deliver product X
to develop product X	essor Y	multicore processor Y	schedulability analysis equations	

SBESC 2019 The consequences of analyzing timing of software executing on multicores using documentation Voice of the customer: We need product X to use the new multicore time processor Y' Buv Read Create Deliver Project Create Deliver Buy Read model of multidata product product starts: data model of multihardware and χ sheets core We hardware and X sheets core of develop procof want develop procschedulability multicore essor multicore schedulability to essor Y' analysis processor develop analysis Y processor Y' equations product Y equations Х

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New multicore
processor Y
becomes
available

time

New multicore	
processor Y	
becomes	time
available	

Academic researcher create model of hardware and develop schedulability analysis equations for Y

New multico processor Y becomes available		New multicore processor Y' becomes available	time
	Academic researcher create model of hardware and develop schedulability analysis equations for		

New multicore processor Y becomes available	New multico processor Y becomes available		time
rese creat mod hard deve sche anal	el of ware and elop edulability	Academic researcher create model of hardware and develop schedulability analysis equations for Y'	

New multico processor Y becomes available		New multicor processor Y' becomes available		New multicore processor Y" becomes available	time
	Academic researcher create model of hardware an develop schedulabilit analysis equations fo	y	Academic researcher create model of hardware an develop schedulabilit analysis equations fo	ty	

New multicore processor Y becomes available	New multice processor N becomes available		New multico processor Y' becomes available	-	time
re cr m ha de so ai	Academic esearcher reate nodel of ardware and levelop chedulability nalysis equations for Y	Academic researcher create model of hardware ar develop schedulabili analysis equations fo	ty	Academic researcher create model of hardware and develop schedulability analysis equations for Y"	

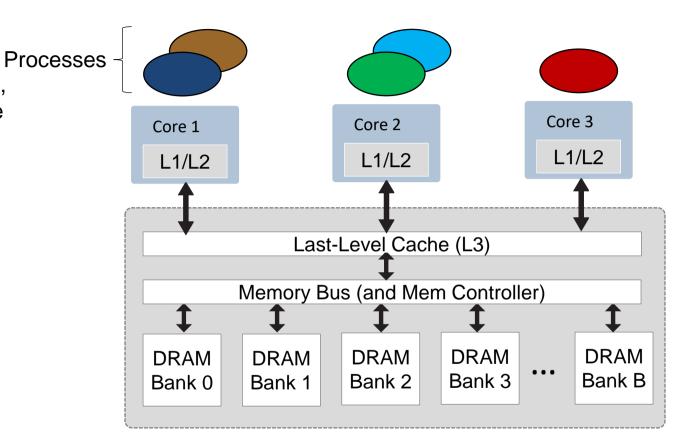
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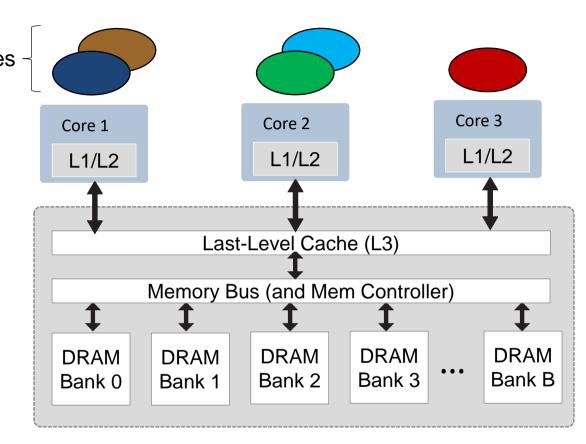


Treating multicore processors as undocumented hardware has the potential to create a model that can be used for processors in the future even for processors that we currently do not know about.

Problem: For each process, compute its response time



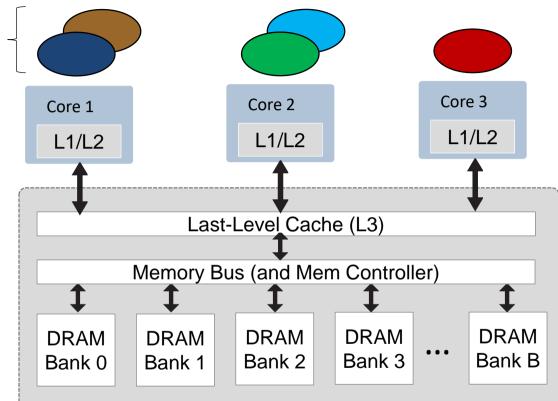
Processes - **Problem:** For each process, compute an upper bound on its response time



Problem: For each process, compute an upper bound on its response time considering contention for resources in the memory system

and

that resources in the memory system are undocumented.

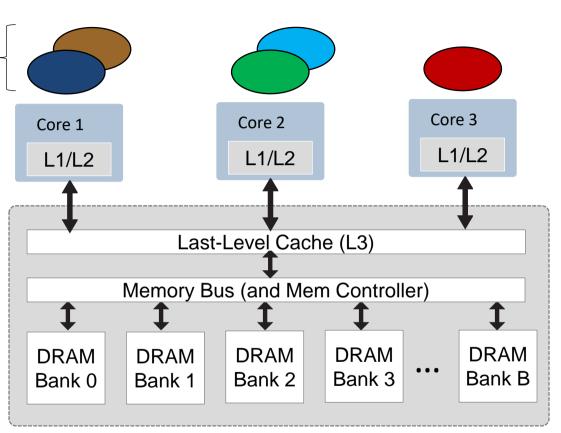


Problem: For each process, compute an upper bound on its response time considering contention for resources in the memory system

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Q: How can we analyze timing of a system when we do not know how the system works?



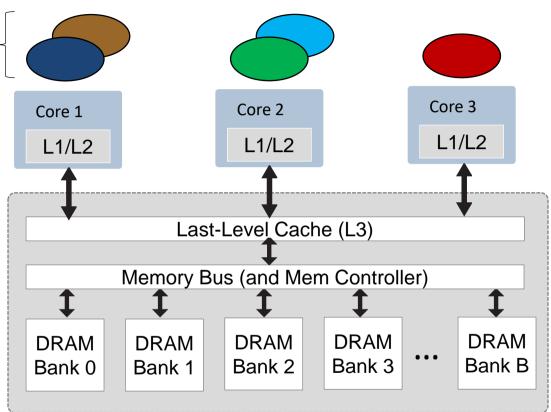
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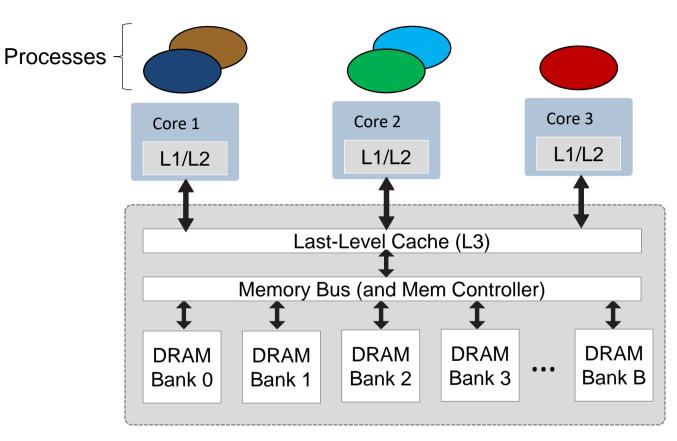
that resources in the memory system are undocumented.

Q: How can we analyze timing of a system when we do not know how the system works?

A: Create abstraction that describes effect of undocumented h/w.



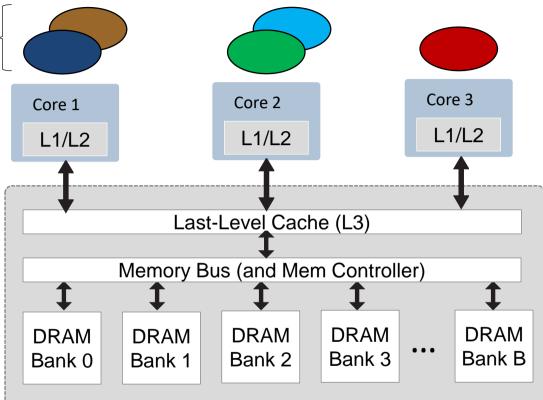
Big Research Questions



Big Research Questions

Q1: What is a good abstraction that describes the effect of undocumented hardware?

Q2: How to create a schedulability analysis that uses this abstraction?



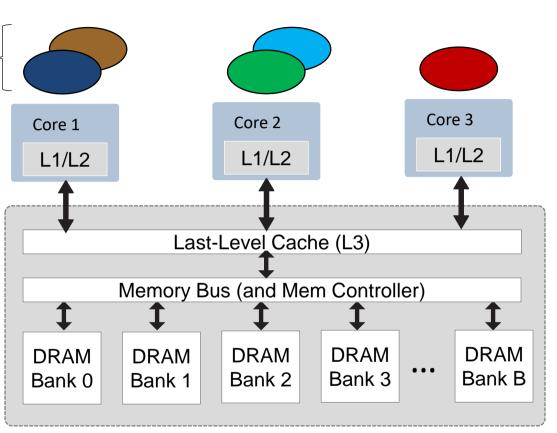
Big Research Questions

Q1: What is a good abstraction that describes the effect of undocumented hardware?

Q2: How to create a schedulability analysis that uses this abstraction?

Before discussing them, let us discuss:

- 1. Other approaches
- 2. General ideas for abstractions in other disciplines



Ignore timing requirements

Ignore timing requirements

Ignore timing aspects of memory system

Ignore timing requirements

Ignore timing aspects of memory system Disable all processor cores except one

Ignore timing requirements

Ignore timing aspects of memory system Disable all processor cores except one Use simple processor and run heavy computations on GPU

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Build your own processor (ASIC)

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Ignore timing aspects of memory system Disable all processor cores except one Use simple processor and run heavy computations on GPU

Build your own processor (ASIC)

Build your own processor (FPGA)

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Ignore timing requirements

Ignore timing aspects of memory system Disable all processor cores except one Use simple processor and run heavy computations on GPU

Build your own processor (ASIC)

Build your own processor (FPGA) Use welldocumented hardware (e.g., RISC-V) and model all resources and create analysis

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[DISTRIBUTION STATEMENT A] Approved for public release and unlimited distribution.

Ignore timing requirements	Ignore timing aspects of memory system	Disable all processor cores except one
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create analysis

Use simple processor and run heavy computations on GPU

Build your own processor (ASIC)

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Ignore timing requirements	Ignore timing aspects of memory system	Disable all processor cores except one	Use simple processor and run heavy computations on GPU	Build your own processor (ASIC)		
Build your own processor (FPGA)	Use well- documented hardware (e.g., RISC-V) and model all resources and create analysis	Model some resources and create analysis	Software-based mechanism to improve predictability/iso lation			

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Ignore timing requirements	Ignore timing aspects of memory system	Disable all processor cores except one	Use simple processor and run heavy computations on GPU	Build your own processor (ASIC)
Build your own processor (FPGA)	Use well- documented hardware (e.g., RISC-V) and model all resources and create analysis	Model some resources and create analysis	Software-based mechanism to improve predictability/iso lation	Reorganize program so that at most one program accesses memory at a time

Ignore timing requirements

Ignore timing aspects of memory system

Disable all processor cores except one Use simple processor and run heavy computations on GPU

Build your own processor (ASIC)

Pro: Easy **Con**: Potentially unsafe

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Ignore timing requirements Ignore timing aspects of memory system Disable all processor cores except one Use simple processor and run heavy computations on GPU

Build your own processor (ASIC)

Pro: Easy Con: Lose lots of processing capacity

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Ignore timing requirements

Ignore timing aspects of memory system Disable all processor cores except one Use simple processor and run heavy computations on GPU

Build your own processor (ASIC)

Con: Analyzing timing of a single "task" executing on a GPU is still hard.

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Ignore timing requirements

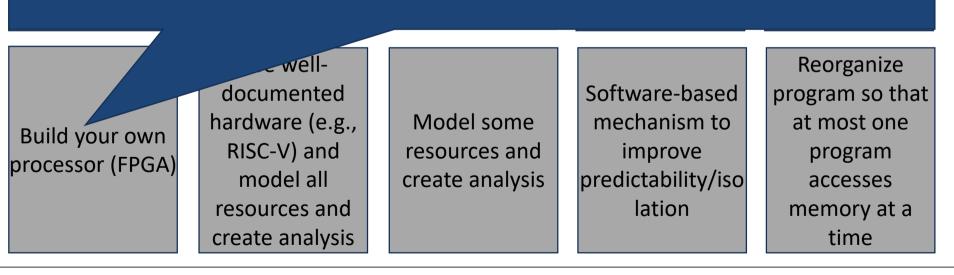
Ignore timing aspects of memory system Disable all processor cores except one Use simple processor and run heavy computations on GPU

Build your own processor (ASIC)

Con: High fixed cost.

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Con: Low clock frequency



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Con: Limits #suppliers. Laborious.

		Use well-			Reorganize
Build your own processor (FPGA)		documented		Software-based	program so that
		hardware (e.g.,	Model some	mechanism to	at most one
		RISC-V) and	resources and	improve	program
		model all	create analysis	predictability/iso	accesses
		resources and		lation	memory at a
		create analysis			time

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Con: Laborious. There may be many resources for which documentation does not exist.

Build your own processor (FPGA)
processor (FPGA)

Use welldocumented hardware (e.g., RISC-V) and model all resources and create analysis

Model some resources and create analysis Software-based mechanism to improve predictability/iso lation Reorganize program so that at most one program accesses memory at a time

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Examples: Cache coloring, Cache locking, Bank coloring, MemGuard, TLB coloring.Con: Requires changes to operating system. Only work for some resources; there are many resources for which there is no isolation mechanism.

Build your own processor (FPGA)	Use well- documented hardware (e.g., RISC-V) and model all resources and create analysis	Model some resources and create analysis	Software-based mechanism to improve predictability/iso lation	Reorganize program so that at most one program accesses memory at a time
------------------------------------	--	--	---	--

Examples: PREM, Linkoping@RTSS07.

Con: Laborious. Requires a local memory that is large enough to store working set. Difficult to prove that no memory accesses occurs in certain phases.

Build your own processor (FPGA)	Use well- documented hardware (e.g., RISC-V) and model all resources and create analysis	Model some resources and create analysis	Software-based mechanism to improve predictability/iso lation	Reorganize program so that at most one program accesses memory at a time
------------------------------------	--	--	---	--

Processes -

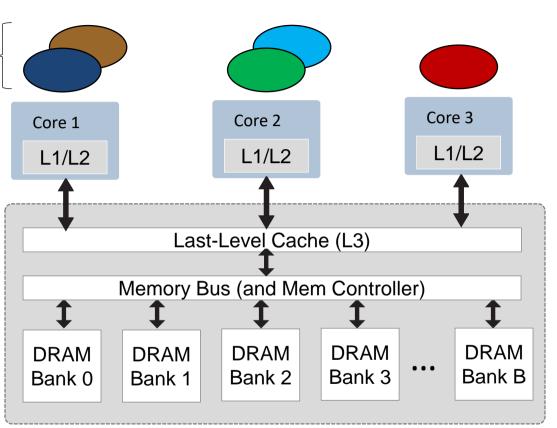
Big Research Questions

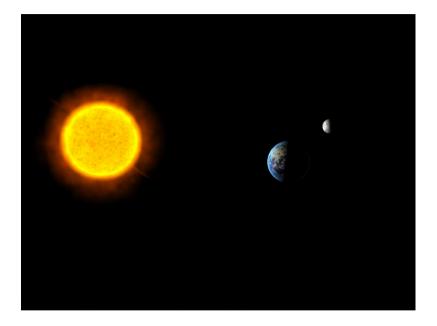
Q1: What is a good abstraction that describes the effect of undocumented hardware?

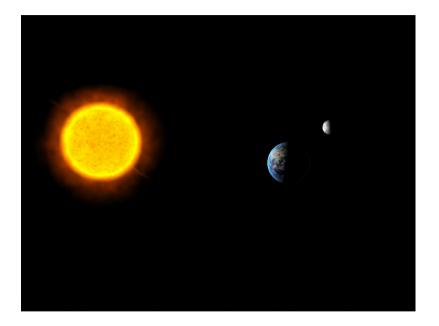
Q2: How to create a schedulability analysis that uses this abstraction?

Before discussing them, let us discuss:

- 1. Other approaches (DONE)
- 2. General ideas for abstractions in other disciplines

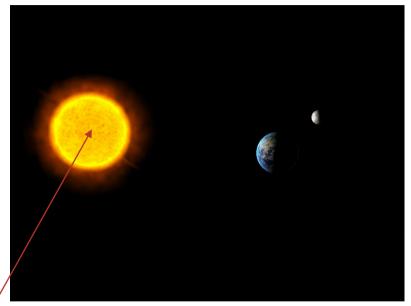






Not drawn to scale

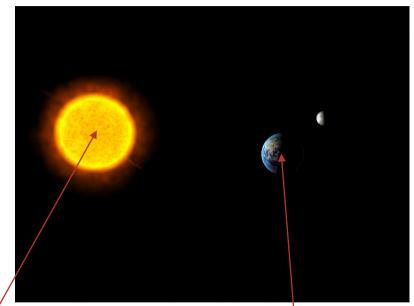
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This body has many atoms

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General ideas for abstractions in other disciplines

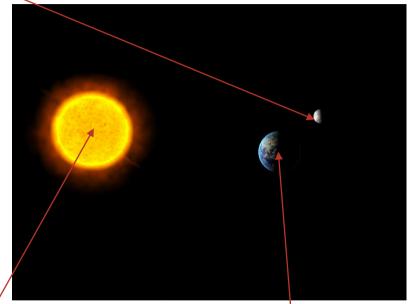


This body has many atoms This body has many atoms

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General ideas for abstractions in other disciplines

This body also has many atoms

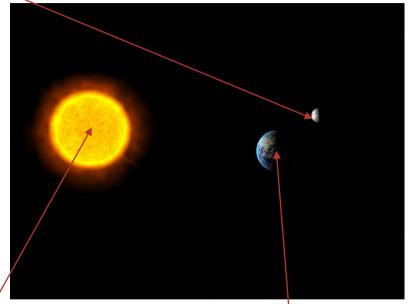


This body has many atoms This body has many atoms

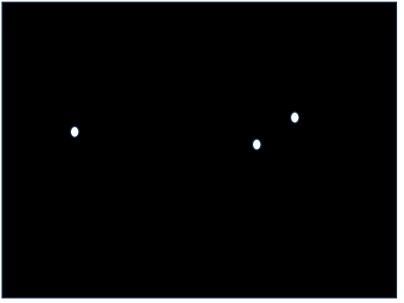
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General ideas for abstractions in other disciplines

This body also has many atoms



We describe each body as a single point mass

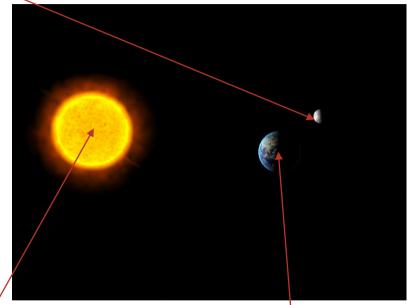


This body has many atoms This body has many atoms

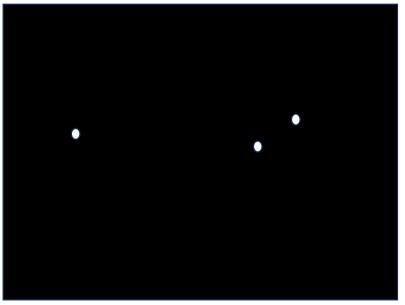
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General ideas for abstractions in other disciplines

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We describe each body as a single point mass



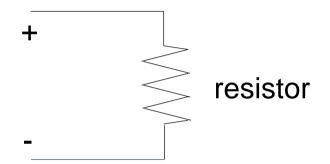
This body has many atoms This body has many atoms

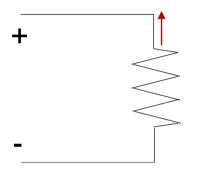
Describe each body with only as many parameters that we need for the analysis that we want to do.

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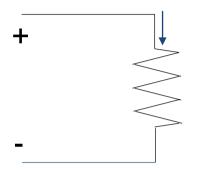
General ideas for abstractions in other disciplines





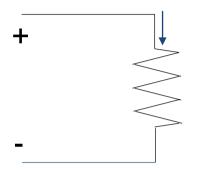
How many electrons per time unit are flowing here?

General ideas for abstractions in other disciplines



How much current is flowing here?

General ideas for abstractions in other disciplines



How much current is flowing here?

Ask questions about the aggregate that you care about.

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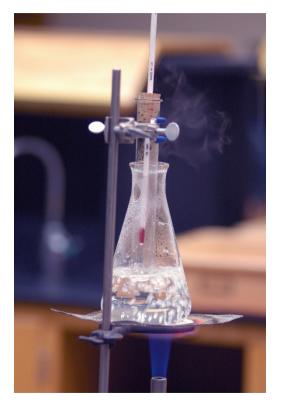


For **each** of these 10²⁴ water molecules, how fast does this water molecule move?

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General ideas for abstractions in other disciplines

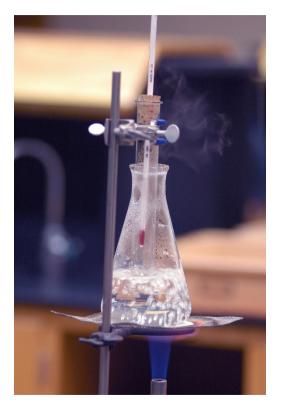


What is the water temperature?

Ask questions about the aggregate that you care about.

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General ideas for abstractions in other disciplines



What is the water temperature?

If possible: Describe a system with quantities that you can measure.

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General ideas for abstractions in other disciplines

1. Describe a system with parts

2. Describe each part with an abstraction

3. Obtain specific values of the abstraction (e.g., using measurements) for each part

4. Ask questions: calculate the answer to the questions

General ideas for abstractions

1. Describe a system with parts

2. Describe each part with an abstraction

3. Obtain specific values of the abstraction (e.g., using measurements) for each part

4. Ask questions: calculate the answer to the questions

General ideas for abstractions

- Describe a system with parts
 A software system comprises a set of tasks.
- Describe each part with an abstraction Each task is described with a T (period), D (deadline), and C (execution time).
- Obtain specific values of the abstraction (e.g., using measurements) for each part Obtain T from source code. Obtain D from software requirement specification. Obtain C by measuring the execution of the program; then add margin. (or run WCET tool)

4. Ask questions: calculate the answer to the questions Will all deadlines be met if tasks are scheduled by Rate-Monotonic on a single processor?

General ideas for abstractions

- Describe a system with parts
 A software system comprises a set of tasks.
- Describe each part with an abstraction Each task is described with a T (period), D (deadline), and C (execution time). Describe the effect of the memory system on execution speed of a task.
- Obtain specific values of the abstraction (e.g., using measurements) for each part Obtain T from source code. Obtain D from software requirement specification. Obtain C by measuring the execution of the program; then add margin. (or run WCET tool) Obtain parameters (e.g., using measurements)
- 4. Ask questions: calculate the answer to the questions Will all deadlines be met if tasks are scheduled by Rate-Monotonic on a single processor?

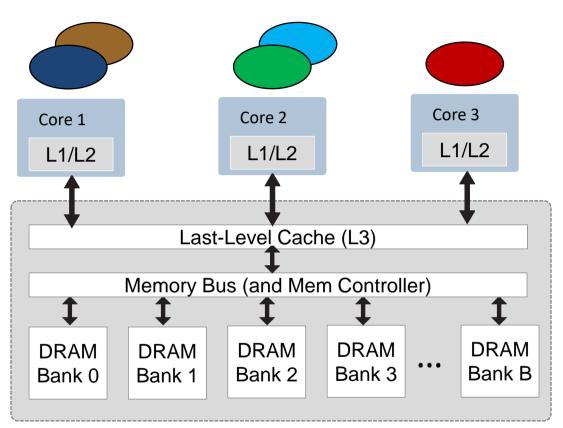
Big Research Questions

Q1: What is a good abstraction that describes the effect of undocumented hardware?

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Before discussing them, let us discuss:

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- 2. General ideas for abstractions in other disciplines (DONE)

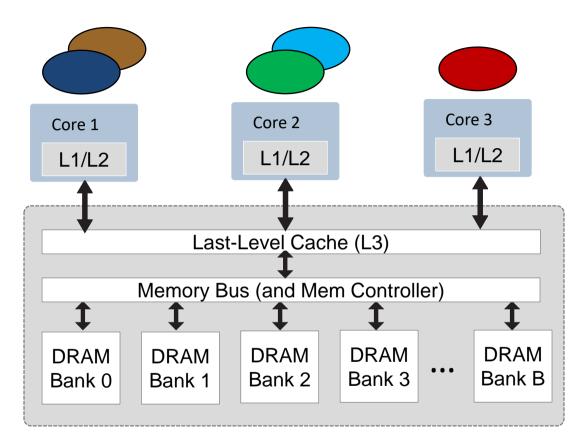


Big Research Questions

Q1: What is a good abstraction that describes the effect of undocumented hardware?

Q2: How to create a schedulability analysis that uses this abstraction?

Let us discuss Q1.

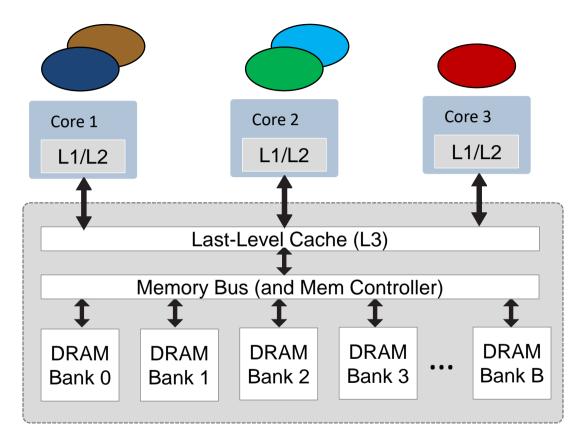


Big Research Questions

Q1: What is a good abstraction that describes the effect of undocumented hardware?

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What are the requirements of a good abstraction?

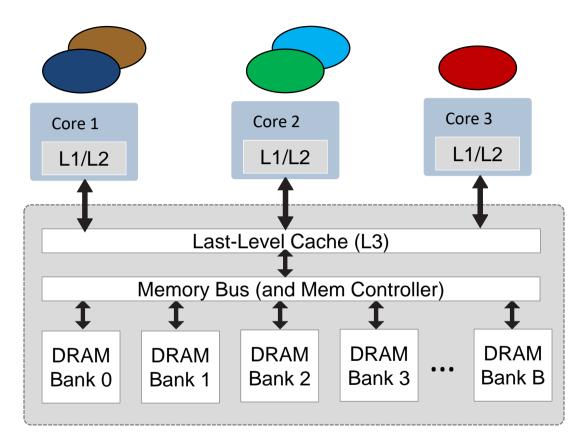


Big Research Questions

Q1: What is a good abstraction that describes the effect of undocumented hardware?

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- What are the requirements of a good abstraction?
 - 1. It should be as small as possible (few numbers; few bits)

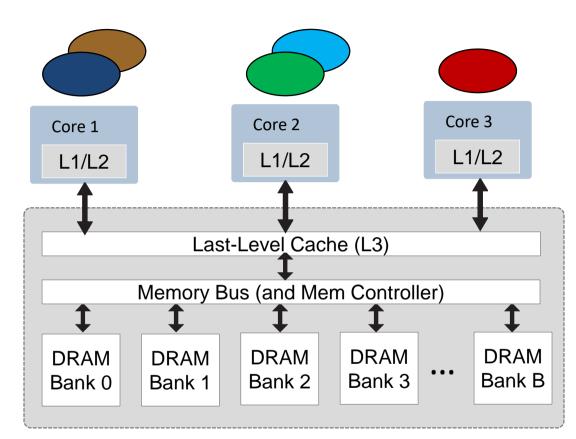


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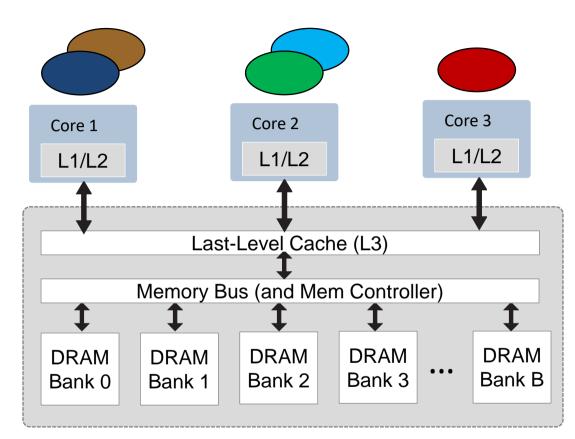


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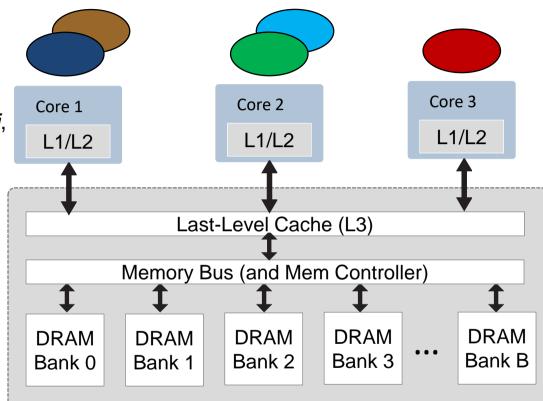
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- What are the requirements of a good abstraction?
 - 1. It should be as small as possible (few numbers; few bits)
 - 2. It should allow us to do prediction/ analysis that we care about
 - 3. Given a system, it should be possible to find the abstraction (through measurements or lower-level analysis)



Considerations in creating an abstraction for multicore

Let speed(i,t) denote the speed of execution of task *i* at time *t*. Let cor(i,t)denote the set of tasks, other than task *i*, that executes at time *t*.

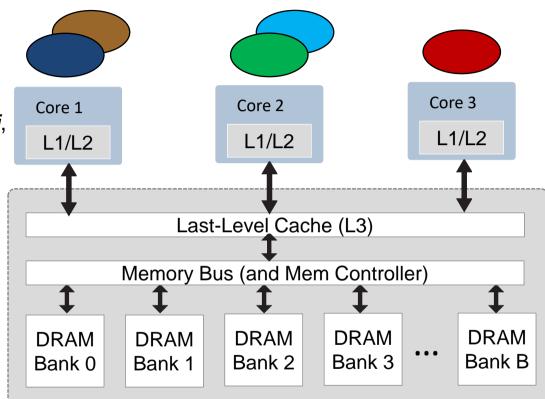


SBESC 2019 Considerations in creating an abstraction for multicore

Let *speed*(*i*,*t*) denote the speed of execution of task *i* at time *t*. Let cor(i,t)denote the set of tasks, other than task *i*. that executes at time t.

One abstraction could be:

$$\frac{1}{+|cor(i,t)|} \le speed(i,t) \le$$



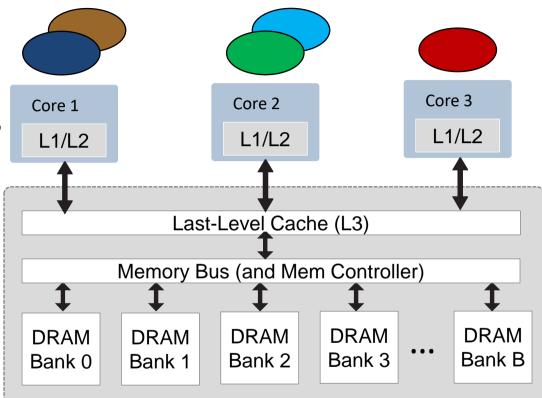
Let speed(i,t) denote the speed of execution of task *i* at time *t*. Let cor(i,t)denote the set of tasks, other than task *i*, that executes at time *t*.

One abstraction could be:

 $\frac{1}{1 + |cor(i,t)|} \le speed(i,t) \le 1$

Drawback of abstraction:

- Does not reflect that different corunners can have different effect on task *i*.



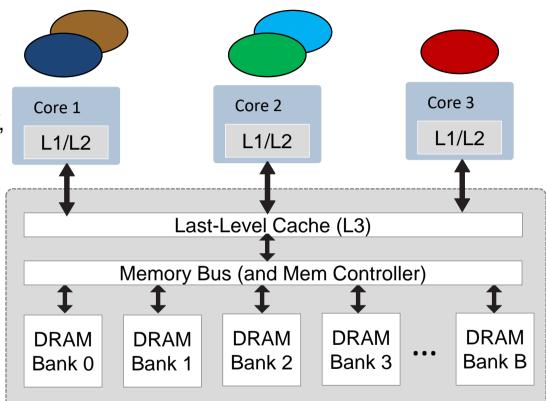
Let speed(i,t) denote the speed of execution of task *i* at time *t*. Let cor(i,t)denote the set of tasks, other than task *i*, that executes at time *t*.

One abstraction could be:

 $1 - k \times |cor(i, t)| \leq speed(i, t) \leq 1$

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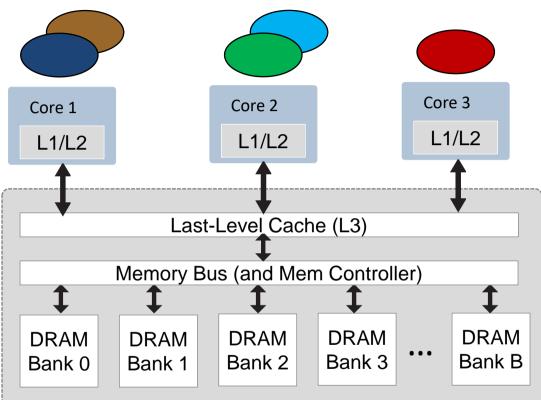
Let speed(i,t) denote the speed of execution of task *i* at time *t*. Let cor(i,t)denote the set of tasks, other than task *i*, that executes at time *t*.

One abstraction could be:

$$\frac{w_i}{1 + \sum_{j \mid j \in cor(i,t)} w_{i,j}} \le speed(i,t) \le 1$$

Drawback of abstraction:

In reality, the speed can be super -additive or sub-additive (not reflected in the above).



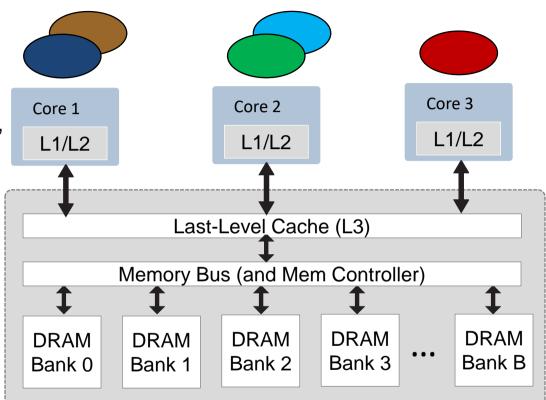
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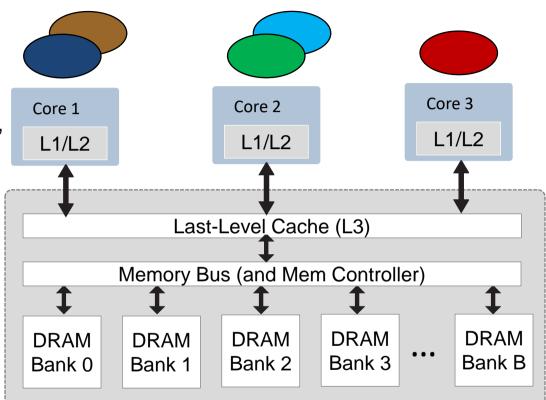
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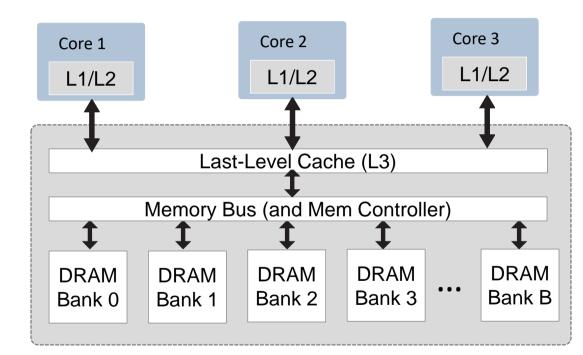
 $\frac{w_i}{1 + e^{\sum_{j \mid j \in cor(i,t)} w_{i,j}}} \le speed(i,t) \le 1$

Drawback of abstraction:

In reality, the speed can be super -additive or sub-additive (not reflected in the above).

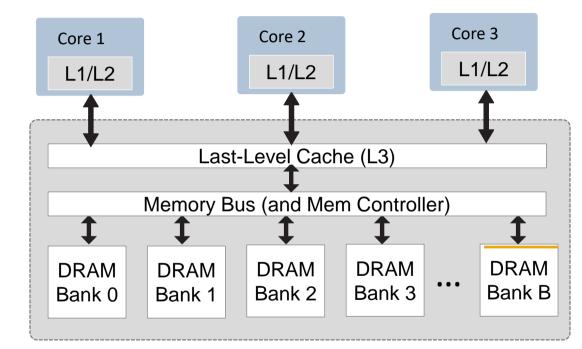


Why is speed sub-additive?



Why is speed sub-additive?

Consider DRAM bank B and its row buffer.



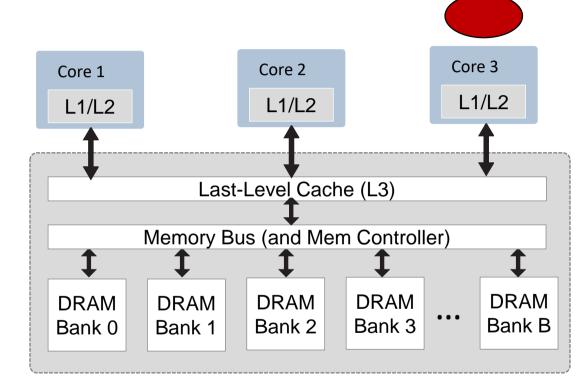
Why is speed sub-additive? Example:

Red task (victim):

1. load address x to register y

2. load address x' to register z

x and x' are in the same row in DRAM bank B' But x and x' are in different columns (different addresses)

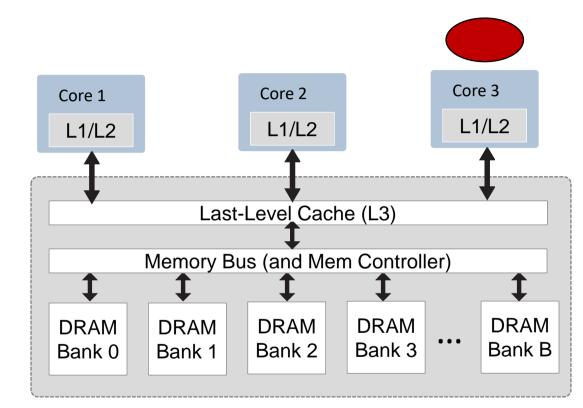


Why is speed sub-additive? Example:

Red task:

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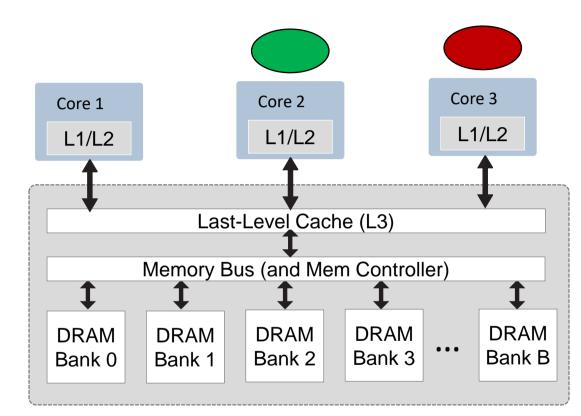
Why is speed sub-additive? Example:

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1. load address a (where a is in same bank as x but in different row)



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Red task:

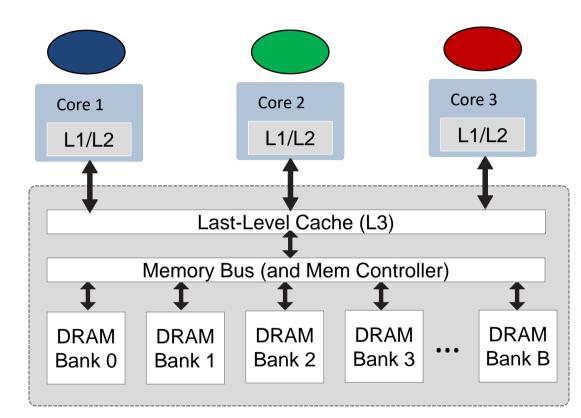
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Blue task:

1. load address b (where b is in same bank as x but in different row)



Why is speed sub-additive? Example:

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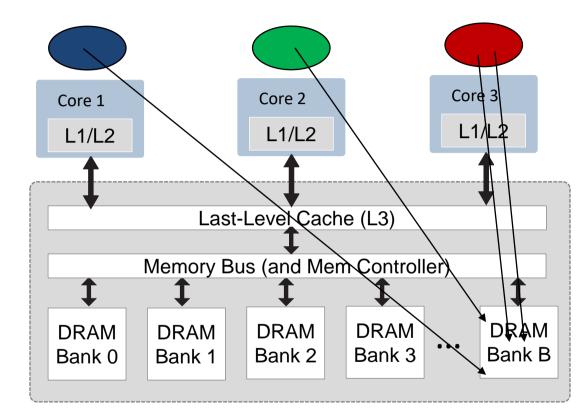
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Red task:

1. load address x to register y

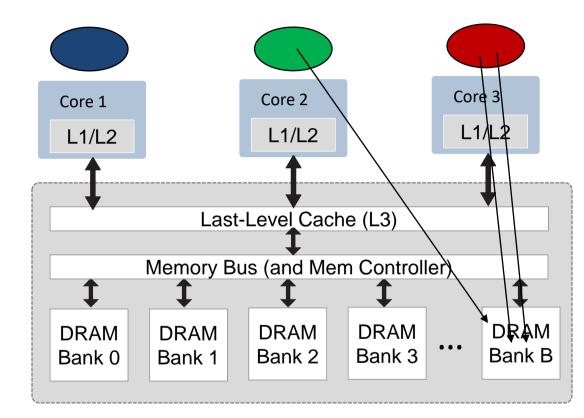
2. load address x' to register z Green task:

1. load address a (where a is in same bank as x but in different row)

Blue task:

1. load address b (where b is in same bank as x but in different row)

Observation: Green can evict Red's data in the row buffer.



Why is speed sub-additive? Example:

Red task:

1. load address x to register y

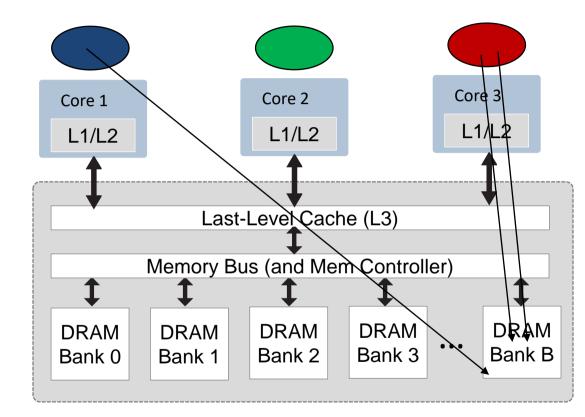
2. load address x' to register z Green task:

1. load address a (where a is in same bank as x but in different row)

Blue task:

1. load address b (where b is in same bank as x but in different row)

Observation: Blue can evict Red's data in the row buffer.



Why is speed sub-additive? Example:

Red task:

1. load address x to register y

2. load address x' to register z Green task:

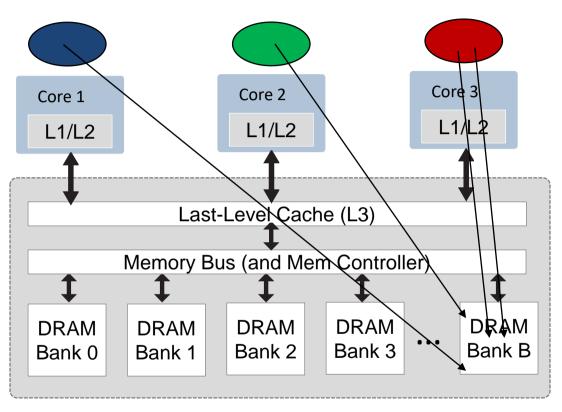
1. load address a (where a is in same bank as x but in different row)

Blue task:

1. load address b (where b is in same bank as x but in different row)

Observation: If Blue has evicted Red's

data in the row buffer, then Green cannot evict it more.



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Why is speed sub-additive? Example:

Red task:

1. load address x to register y

2. load address x' to register z Green task:

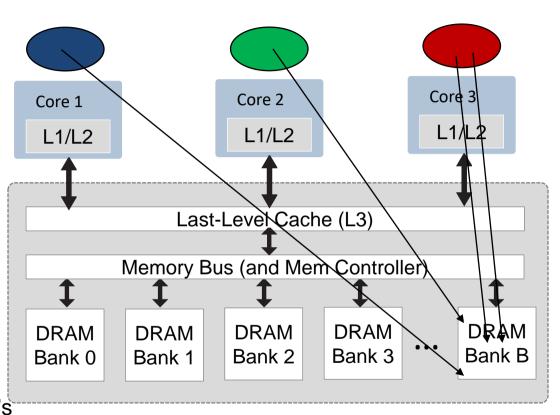
1. load address a (where a is in same bank as x but in different row)

Blue task:

1. load address b (where b is in same bank as x but in different row)

Observation: If Green has evicted Red's

data in the row buffer, then Blue cannot evict it more.



Why is speed sub-additive? Example:

Red task:

1. load address x to register y

2. load address x' to register z Green task:

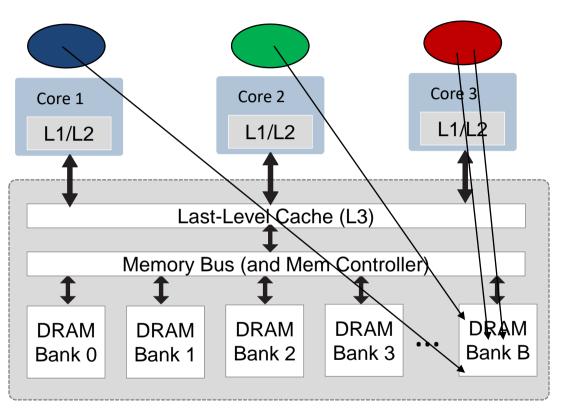
1. load address a (where a is in same bank as x but in different row)

Blue task:

1. load address b (where b is in same bank as x but in different row)

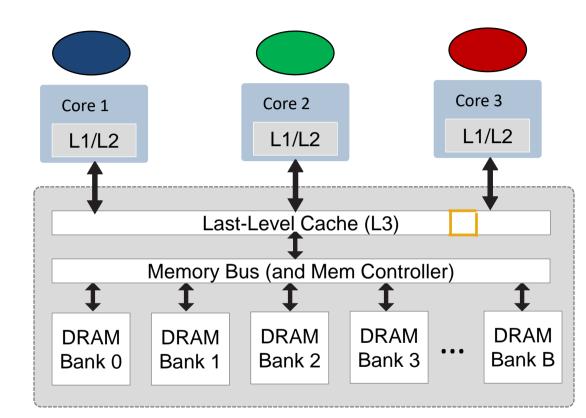
Red experiences a slowdown due to

Blue or Green but the slowdown is not greater by both.



Why is speed super-additive?

Consider Last-Level Cache (L3). Assume associativity = 2. Consider one specific cache set.

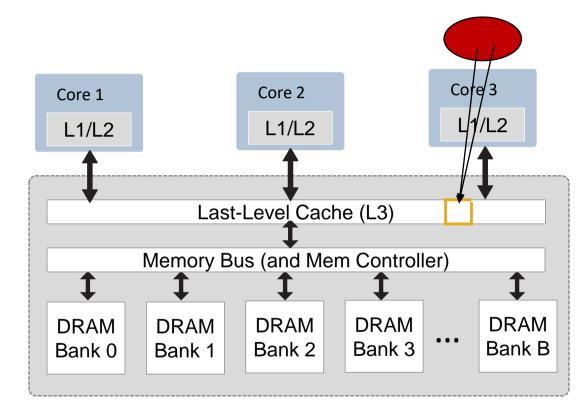


Why is speed super-additive?

Example:

Red task (victim):

- 1. load address x to register y
- 2. load address x to register z



Why is speed super-additive?

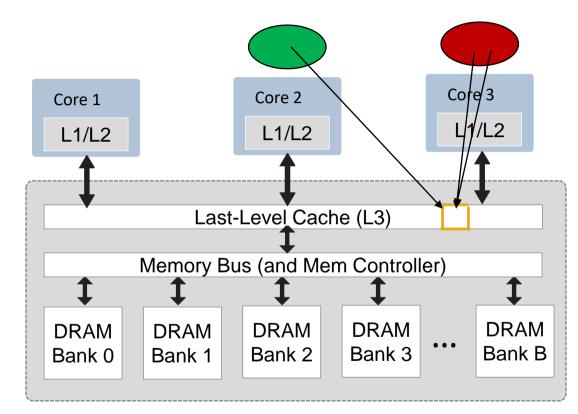
Example:

Red task (victim):

- 1. load address x to register y
- 2. load address x to register z

Green task:

1. load address a (where a is in same cache set x)



Why is speed super-additive?

Example:

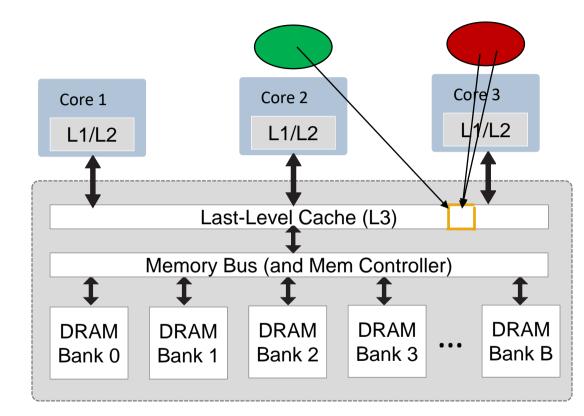
Red task (victim):

- 1. load address x to register y
- 2. load address x to register z

Green task:

1. load address a (where a is in same cache set x)

Observation: Green's data and Red's data fit in the cache. No capacity miss.



Why is speed super-additive?

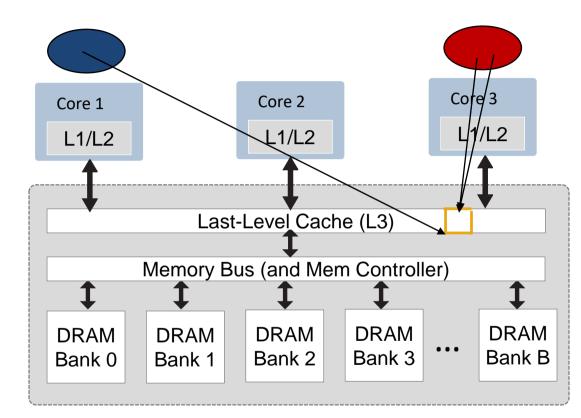
Example:

Red task (victim):

- 1. load address x to register y
- 2. load address x to register z

Blue task:

- 1. load address b (where b is in same cache set x)
- Observation: Blue's data and Red's data fit in the cache. No capacity miss.



Why is speed super-additive?

Example:

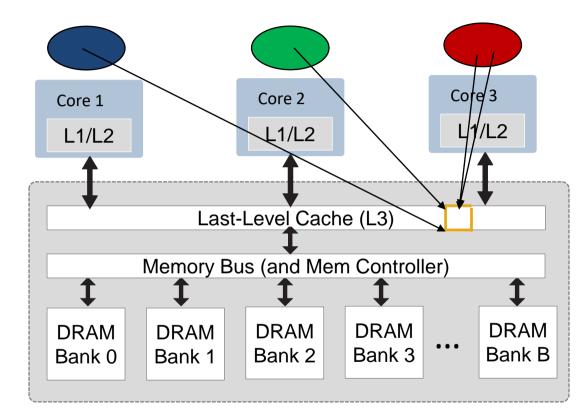
Red task (victim):

- 1. load address x to register y
- 2. load address x to register z Green task:
 - 1. load address a (where a is in same cache set x)

Blue task:

1. load address b (where b is in same cache set x)

Observation: Blue's data, Green's data, and Red's data do not fit in the cache. Capacity miss.



Why is speed super-additive?

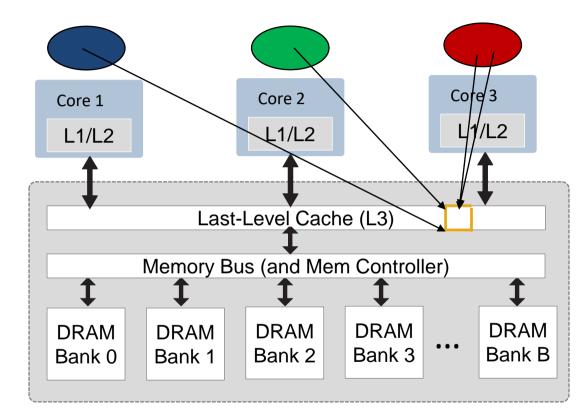
Example:

Red task (victim):

- 1. load address x to register y
- 2. load address x to register z
- Green task:
 - 1. load address a (where a is in same cache set x)

Blue task:

- 1. load address b (where b is in same cache set x)
- Observation: Green alone does not cause slowdown of Red.



Why is speed super-additive?

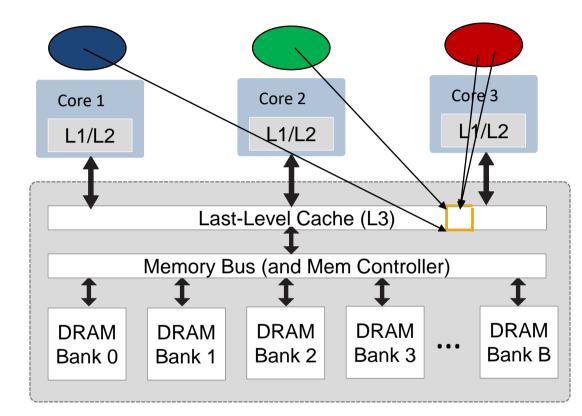
Example:

Red task (victim):

- 1. load address x to register y
- 2. load address x to register z reen task:
- Green task:
 - 1. load address a (where a is in same cache set x)

Blue task:

- 1. load address b (where b is in same cache set x)
- Observation: Blue alone does not cause slowdown of Red.



Why is speed super-additive?

Example:

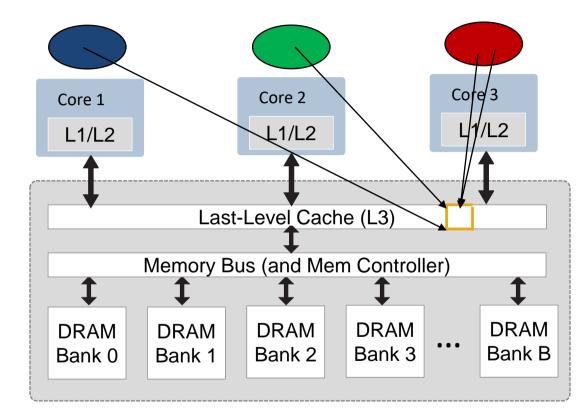
Red task (victim):

- 1. load address x to register y
- 2. load address x to register z reen task:
- Green task:
 - 1. load address a (where a is in same cache set x)

Blue task:

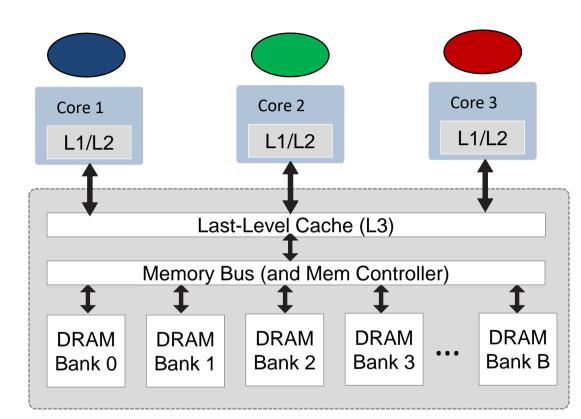
1. load address b (where b is in same cache set x)

Observation: But Green and Blue cause slowdown of Red.



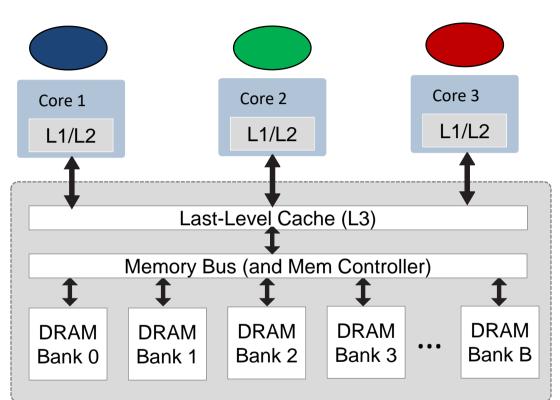
Speed of execution of a task as a function of co-runners can be either

- (i) Additive
- (ii) Sub-additive
- (iii) Super-additive



Speed of execution of a task as a function of co-runners can be either

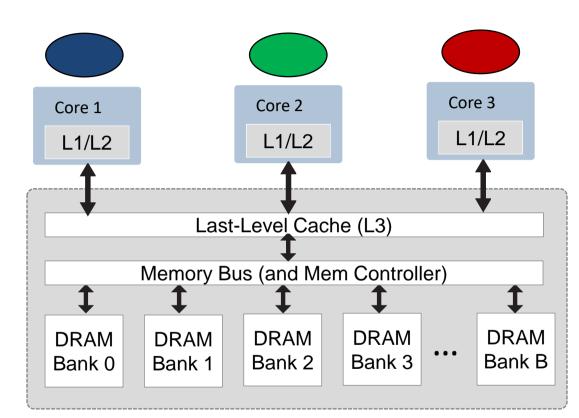
- (i) Additive
- (ii) Sub-additive
- (iii) Super-additive



If speed is not additive, how can we describe speed as a function of co-runners?

Speed of execution of a task as a function of co-runners can be either

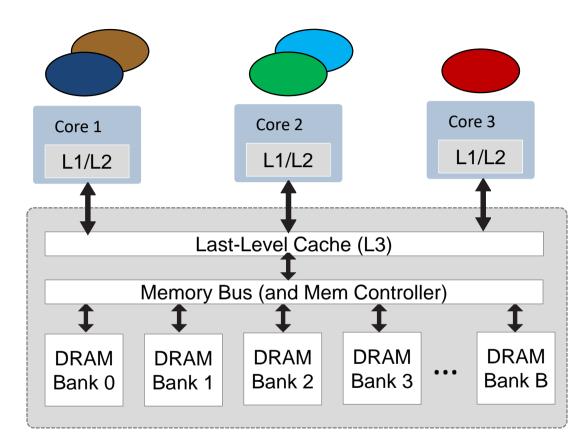
- (i) Additive
- (ii) Sub-additive
- (iii) Super-additive



For each task: Enumerate the set of possible co-runner set.

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Main idea: For each task *i*, for each co-runner set of task *i* do $lowerboundspeed_i^{cor}$ $\leq speed(i,t) \leq 1$



For each task: Enumerate the set of possible co-runner set.

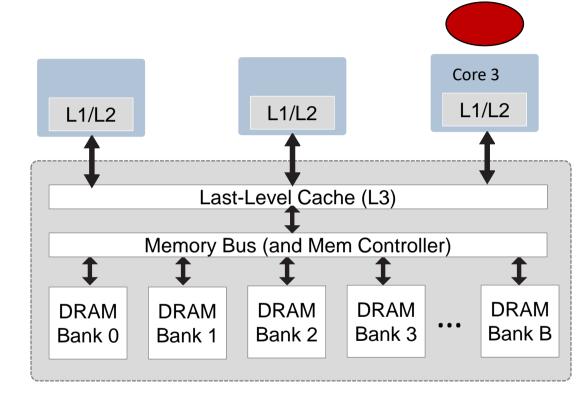
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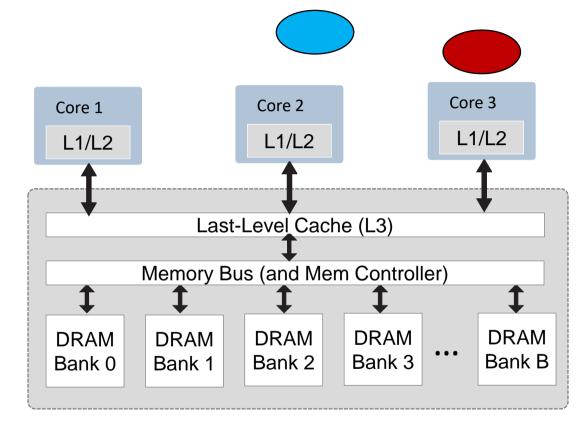
Describing resource consumption of Red task

C _{red} =4	
Co-runner set	Speed
{}	1



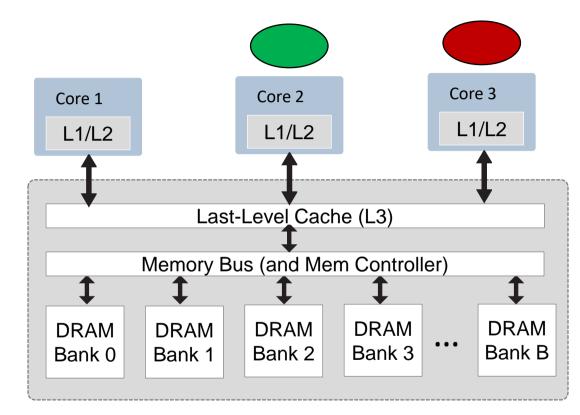
Describing resource consumption of Red task

C _{red} =4	
Co-runner set	Speed
{}	1
{cyan}	0.5



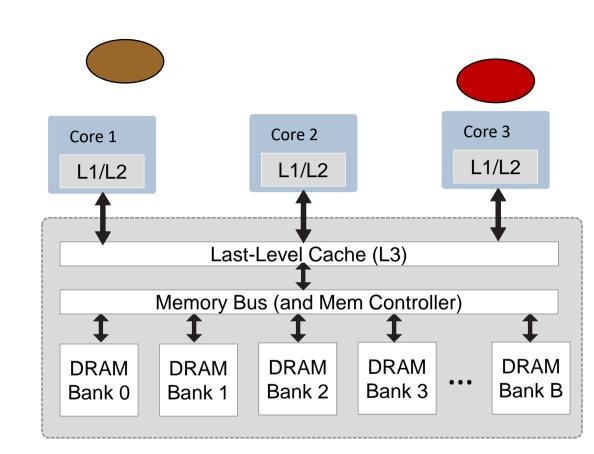
Describing resource consumption of Red task

C _{red} =4	
Co-runner set	Speed
{}	1
{green}	0.45



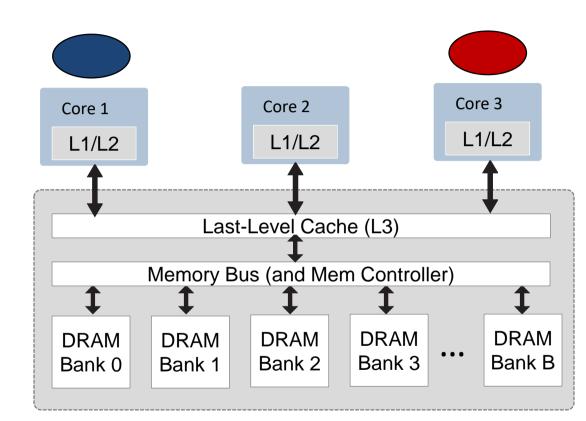
Describing resource consumption of Red task

C _{red} =4	
Co-runner set	Speed
{}	1
{brown}	0.45



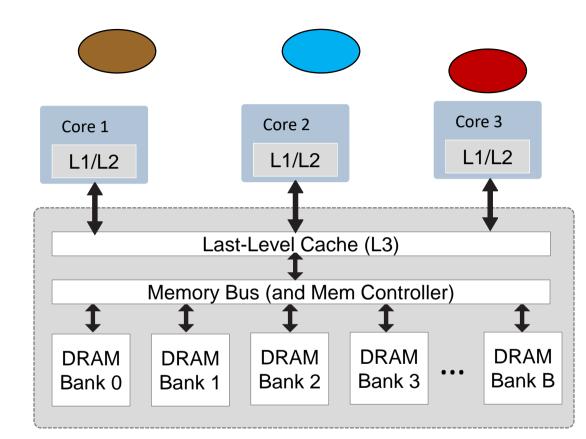
Describing resource consumption of Red task

Speed
1
0.25



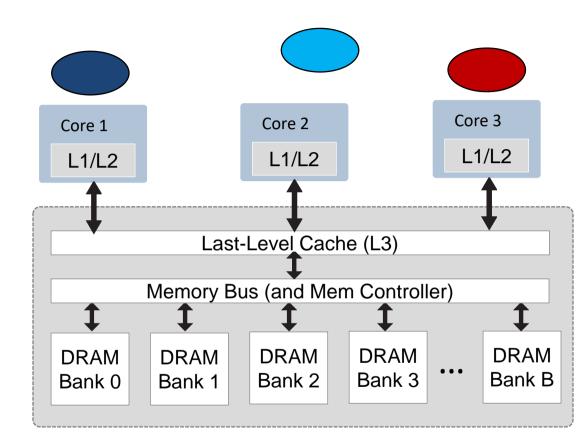
Describing resource consumption of Red task

C _{red} =4	
Speed	
1	
0.18	



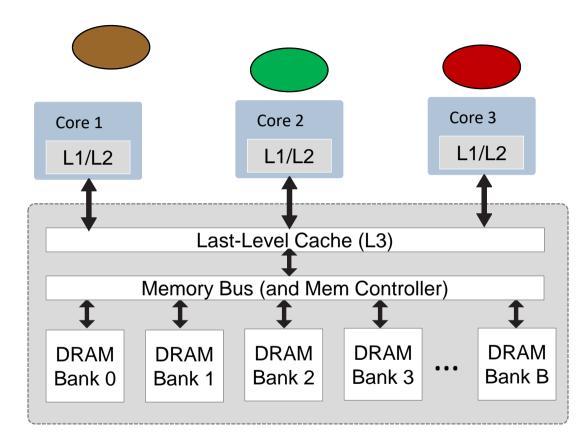
Describing resource consumption of Red task

C _{red} =4				
Speed				
1				
0.12				



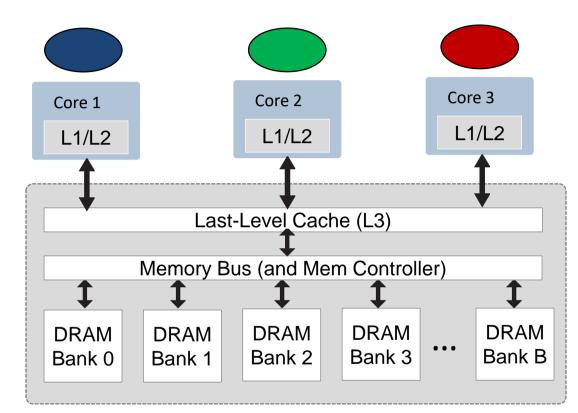
Describing resource consumption of Red task

C _{red} =4	
Co-runner set	Speed
{}	1
{green,brown}	0.13



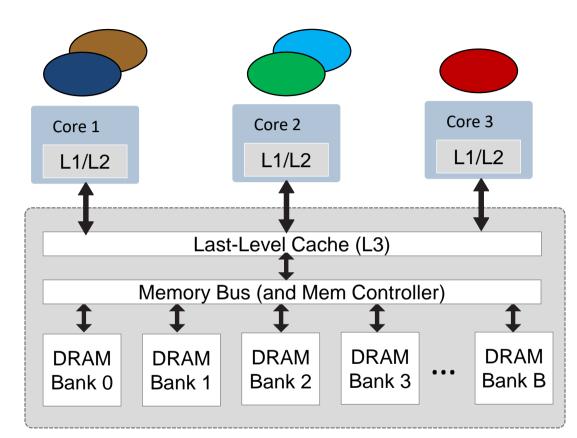
Describing resource consumption of Red task

C _{red} =4			
Co-runner set	Speed		
{}	1		
{green, blue}	0.19		



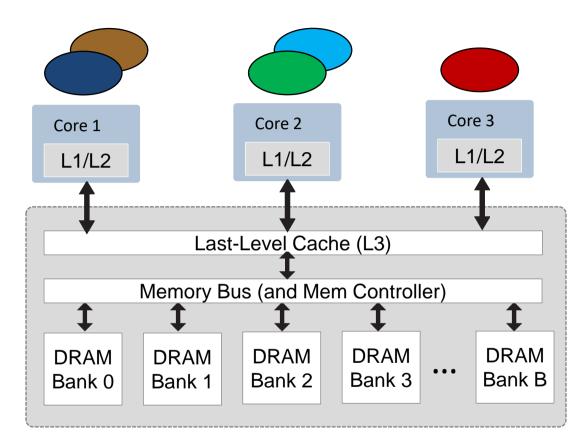
Describing resource consumption of Red task

C _{red} =4			
Co-runner set	Speed		
{}	1		
{cyan}	0.5		
{green}	0.45		
{brown}	0.45		
{blue}	0.25		
{cyan, brown}	0.18		
{cyan, blue}	0.12		
{green,brown}	0.13		
{green, blue}	0.19		



Describing resource consumption of Red task

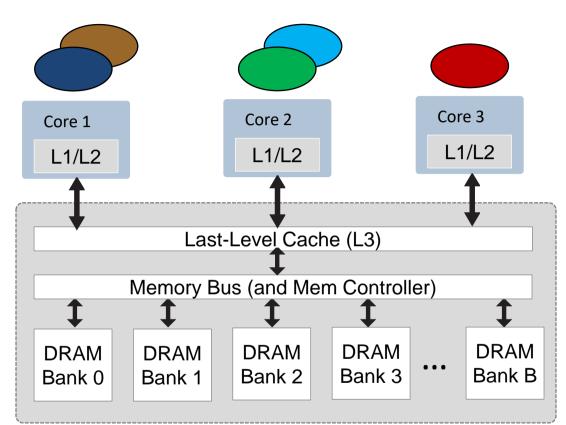
C _{red} =4	
Co-runner set	Speed
{}	1
{cyan}	0.5
{green}	0.45
{brown}	0.45
{blue}	0.25
{cyan, brown}	0.18
{cyan, blue}	0.12
{green,brown}	0.13
{green, blue}	0.19



Describe resource consumption of other tasks analogously.

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Main idea: For each task *i*, for each co-runner set of task *i* do $lowerboundspeed_i^{cor}$ $\leq speed(i,t) \leq 1$



For each task: Enumerate the set of possible co-runner set.

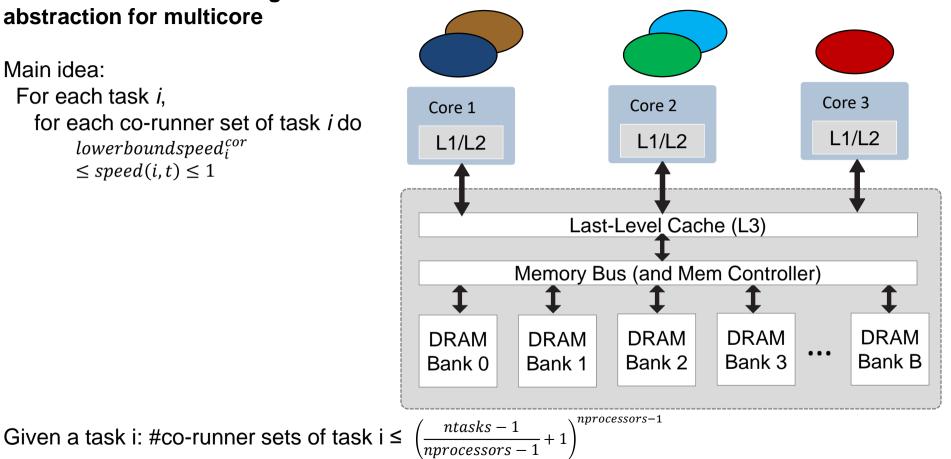
Isn't that exponential? Couldn't this be bad?

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Main idea: For each task *i*, for each co-runner set of task *i* do *lowerboundspeed*^{cor} \leq speed(*i*, *t*) \leq 1

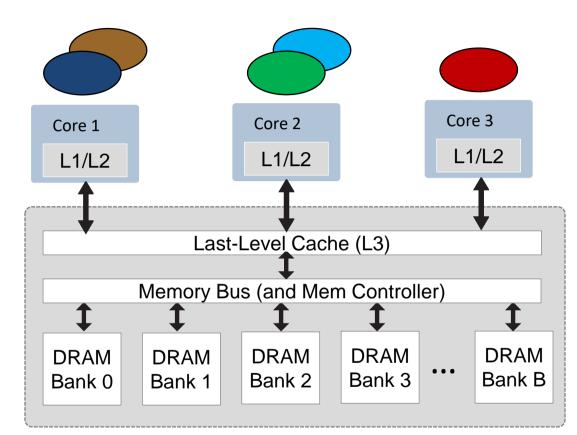


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Main idea: For each task *i*, for each co-runner set of task *i* do $lowerboundspeed_i^{cor}$ $\leq speed(i,t) \leq 1$



Given a task i: #co-runner sets of task i ≤ polynomial

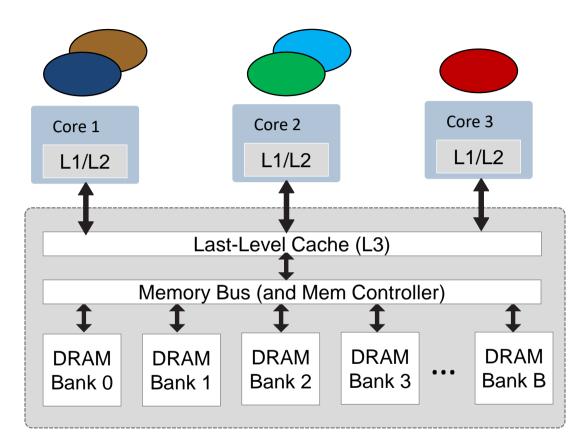
If number of processors is fixed.

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Main idea: For each task *i*, for each co-runner set of task *i* do $lowerboundspeed_i^{cor}$ $\leq speed(i,t) \leq 1$



Given a task i: #co-runner sets of task i ≤ ntasks

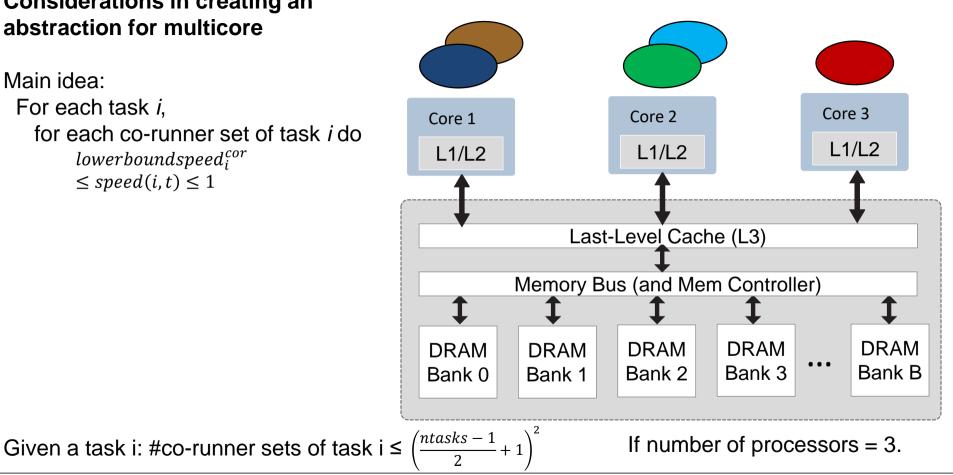
If number of processors = 2.

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Main idea: For each task *i*, for each co-runner set of task *i* do *lowerboundspeed*^{cor} \leq speed(*i*, *t*) \leq 1

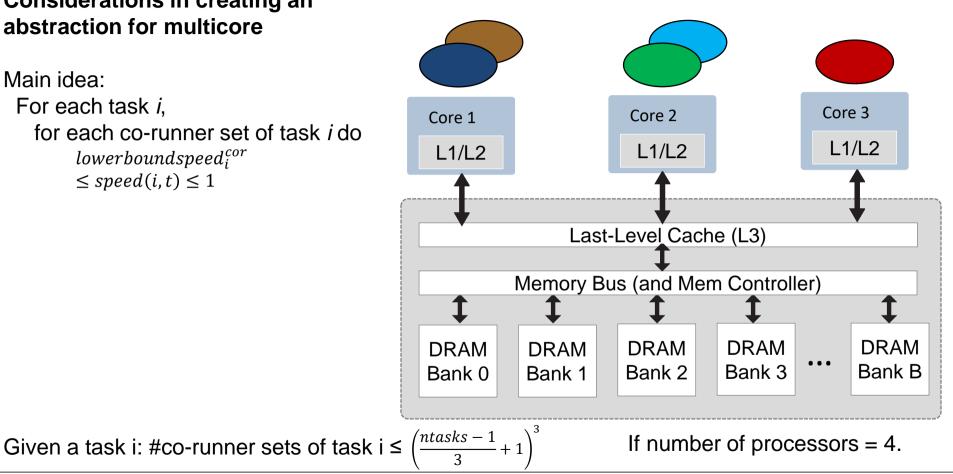


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Main idea: For each task *i*, for each co-runner set of task *i* do *lowerboundspeed*^{cor} \leq speed(*i*, *t*) \leq 1

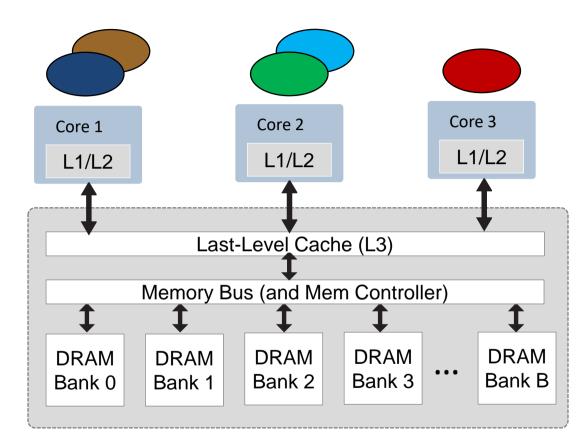


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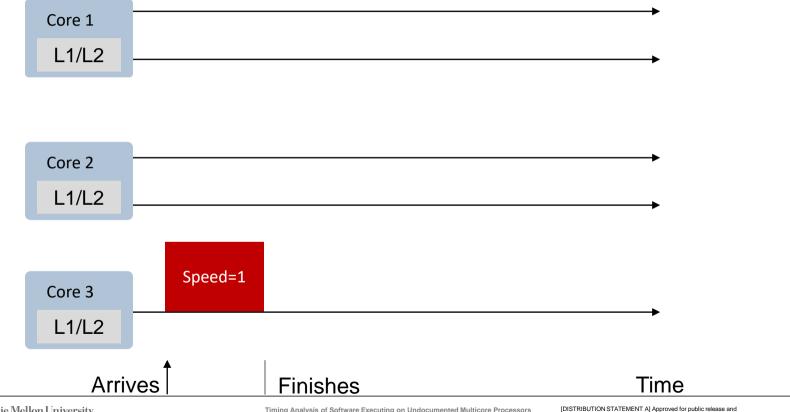
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Given a task *i*: A job of task *i* can experience different co-runner set at different times.



SBESC 2019

How Co-Runners Impact Speed of Execution

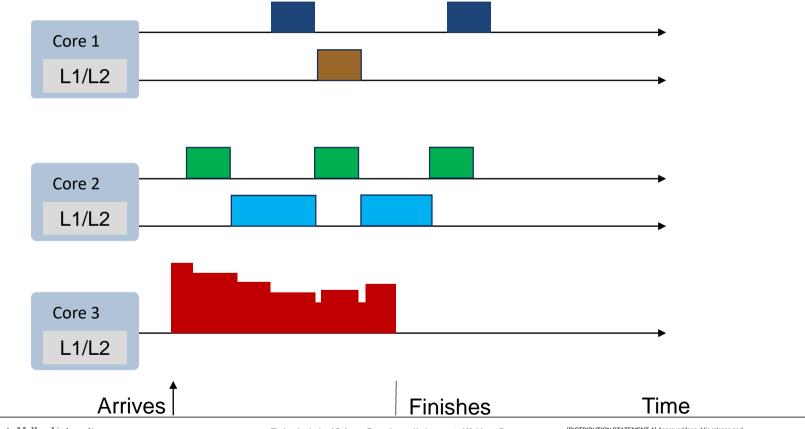


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SBESC 2019

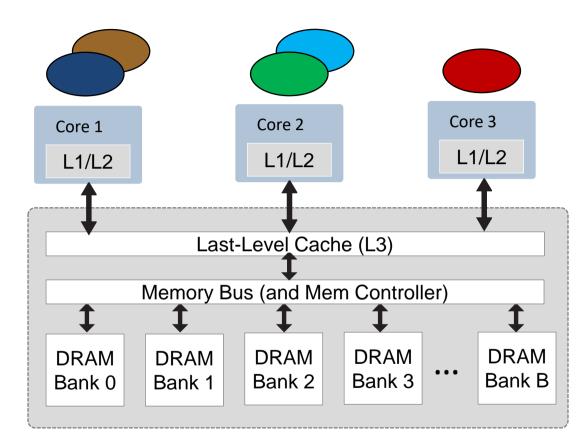
How Co-Runners Impact Speed of Execution



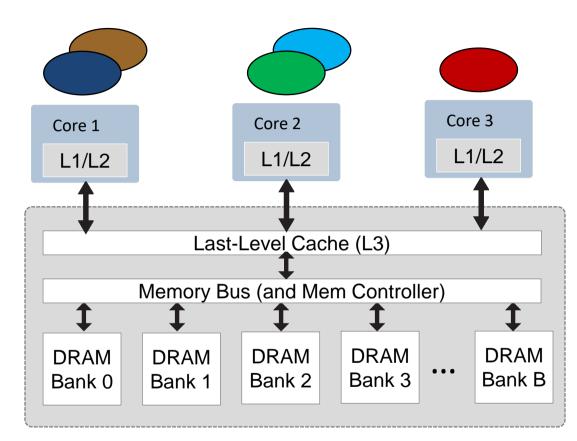
Carnegie Mellon University Software Engineering Institute Timing Analysis of Software Executing on Undocumented Multicore Processors © 2019 Carnegie Mellon University

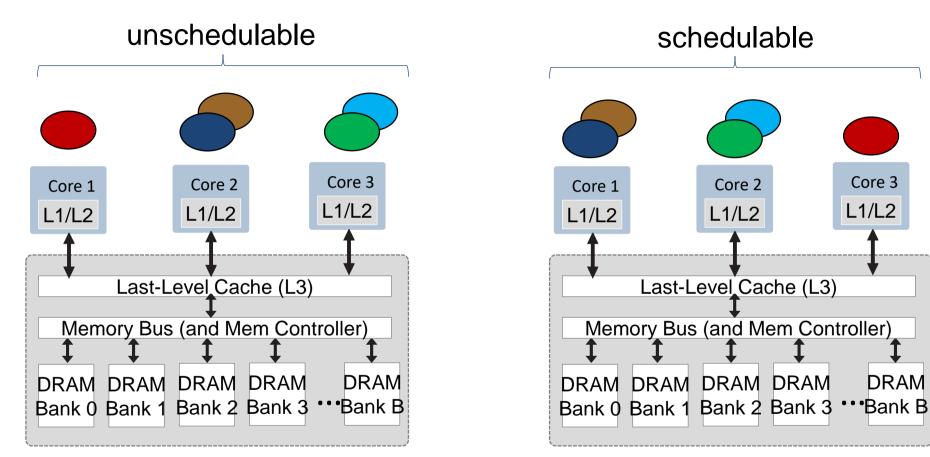
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Given a task *i*: A job of task *i* can experience different co-runner set at different times.

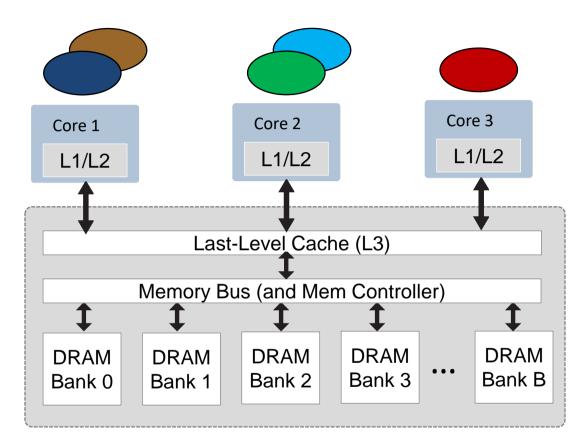


In some computer systems, there are some resources (e.g., memory bus) where the arbitration depends on the processor id of the requestor.

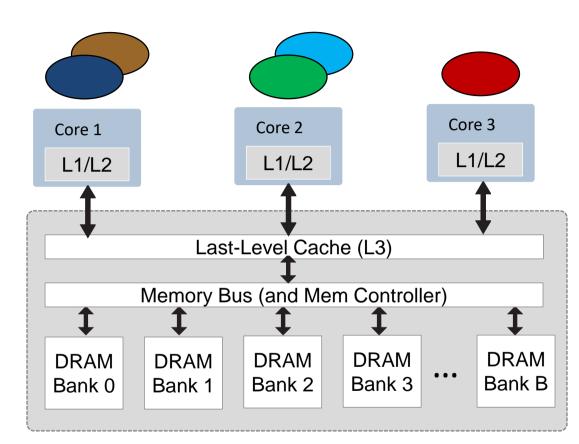




In some computer systems, there are some resources (e.g., memory bus) where the arbitration depends on the processor id of the requestor.

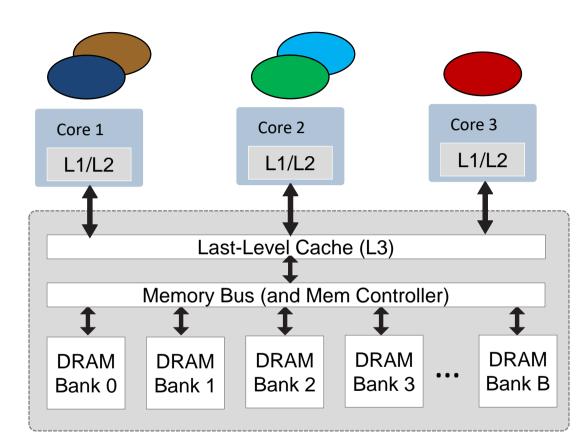


The program behavior may change over time.



The program behavior may change over time.

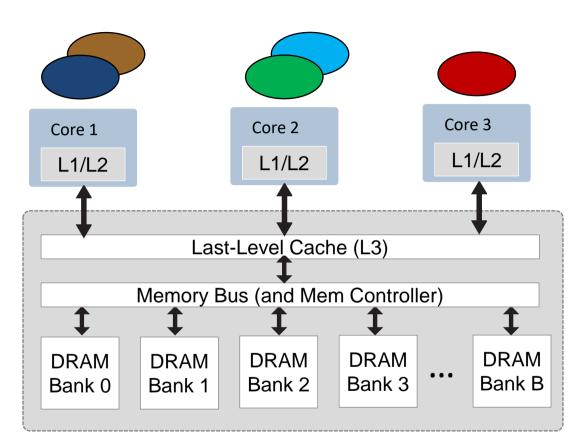
```
while (1) {
   s = wait_until_next_sample()
   update_datastructures(s)
   a = compute_actuation_command()
   actuate_command(a)
```



The program behavior may change over time.

```
while (1) {
   s = wait_until_next_sample()
   update_datastructures(s)
   a = compute_actuation_command()
   actuate_command(a)
```

The program behavior here



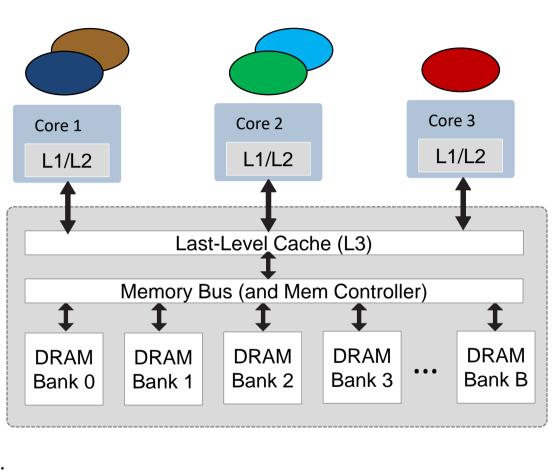
The program behavior may change over time.

```
while (1) {
   s = wait_until_next_sample()
   update_datastructures(s)
   a = compute_actuation_command()
   actuate command(a)
```

The program behavior here

is different from

the program behavior here.



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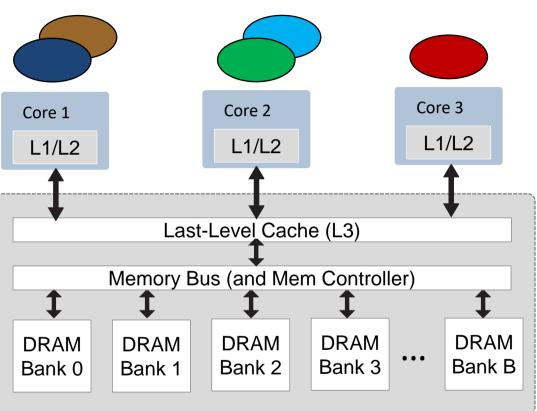
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The program behavior may change over time.

```
while (1) {
   s = wait_until_next_sample()
   update_datastructures(s)
   a = compute_actuation_command()
   actuate_command(a)
```

Describe a task as a sequence of segments where each segment may have different description of lower bound on speed as a function of co-runners.



 $|\tau| = 5$ procs $(\Pi) = \{P_1, P_2\}$ $T_1 = 1.500 \quad D_1 = 1.500 \quad V_1 = \{v_1^1\} \quad \text{prio}_1 = 3 \quad \text{proc}_1 = 1$ = 0.250 pd_1^1 = 0.500 $\text{CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ C_1^1 $T_2 = 2.000 \quad D_2 = 2.000 \quad V_2 = \{v_2^1\} \quad \text{prio}_2 = 2 \quad \text{proc}_2 = 1$ $C_2^1 = 0.250 \text{ pd}_2^1 = 0.500 \text{ CO}_2^1 = \{(\{v_2^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ $T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$ $C_{2}^{1} = 0.250 \text{ pd}_{3}^{1} = 0.500 \text{ CO}_{2}^{1} = \{(\{v_{1}^{1}\}, 1.0), (\{v_{2}^{1}\}, 0.5)\}$ $T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$ $C_4^1 = 0.250 \text{ pd}_4^1 = 0.500 \text{ CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$ $T_5 = 2.250$ $D_5 = 2.250$ $V_5 = \{v_5^1, v_5^2\}$ prio₅ = 1 proc₅ = 2 $C_5^1 = 0.500 \text{ pd}_5^1 = 1.000 \text{ CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$ $C_5^2 = 0.125 \text{ pd}_5^2 = 0.500 \text{ CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$

 $|\tau| = 5$ $procs(\Pi) = \{P_1, P_2\}$ $T_1 = 1.500 \quad D_1 = 1.500 \quad V_1 = \{v_1^1\} \quad \text{prio}_1 = 3 \quad \text{proc}_1 = 1$ = 0.250 pd_1^1 = 0.500 $\text{CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ C^1 $T_2 = 2.000 \quad D_2 = 2.000 \quad V_2 = \{v_2^1\} \quad \text{prio}_2 = 2 \quad \text{proc}_2 = 1$ $C_2^1 = 0.250 \text{ pd}_2^1 = 0.500 \text{ CO}_2^1 = \{(\{v_2^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ $T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$ $C_{2}^{1} = 0.250 \text{ pd}_{3}^{1} = 0.500 \text{ CO}_{2}^{1} = \{(\{v_{1}^{1}\}, 1.0), (\{v_{2}^{1}\}, 0.5)\}$ $T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$ $C_4^1 = 0.250 \text{ pd}_4^1 = 0.500 \text{ CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$ $T_5 = 2.250$ $D_5 = 2.250$ $V_5 = \{v_5^1, v_5^2\}$ prio₅ = 1 proc₅ = 2 $C_5^1 = 0.500 \text{ pd}_5^1 = 1.000 \text{ CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$ $C_5^2 = 0.125 \text{ pd}_5^2 = 0.500 \text{ CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$

5 Task

2 processors

$$|\tau| = 5$$
 procs $(\Pi) = \{P_1, P_2\}$

$$\begin{array}{lll} T_2 &= 2.000 & D_2 &= 2.000 & V_2 = \{v_2^1\} & \text{prio}_2 = 2 & \text{proc}_2 = 1 \\ C_2^1 &= 0.250 & \text{pd}_2^1 &= 0.500 & \text{CO}_2^1 = \{(\{v_3^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \end{array}$$

$$T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$$

$$C_3^1 = 0.250 \quad \text{pd}_3^1 = 0.500 \quad \text{CO}_3^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 0.5)\}$$

$$T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$$

$$C_4^1 = 0.250 \quad \text{pd}_4^1 = 0.500 \quad \text{CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$$

$$T_5 = 2.250 \quad D_5 = 2.250 \quad V_5 = \{v_5^1, v_5^2\} \quad \text{prio}_5 = 1 \quad \text{proc}_5 = 2$$

$$C_5^1 = 0.500 \quad \text{pd}_5^1 = 1.000 \quad \text{CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$$

$$C_5^2 = 0.125 \quad \text{pd}_5^2 = 0.500 \quad \text{CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$$

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 $|\tau| = 5$ procs $(\Pi) = \{P_1, P_2\}$

$$T_1 = 1.500 \quad D_1 = 1.500 \quad V_1 = \{v_1^1\} \quad \text{prio}_1 = 3 \quad \text{proc}_1 = 1$$

$$C_1^1 = 0.250 \quad \text{pd}_1^1 = 0.500 \quad \text{CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$$

$$T_2 = 2.000 \quad D_2 = 2.000 \quad V_2 = \{v_2^1\} \qquad \text{prio}_2 = 2 \quad \text{proc}_2 = 1$$

$$C_2^1 = 0.250 \text{ pd}_2^1 = 0.500 \text{ CO}_2^1 = \{(\{v_3^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$$

$$T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$$

$$C_3^1 = 0.250 \quad \text{pd}_3^1 = 0.500 \quad \text{CO}_3^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 0.5)\}$$

$$T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$$

$$C_4^1 = 0.250 \quad \text{pd}_4^1 = 0.500 \quad \text{CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$$

$$T_5 = 2.250 \quad D_5 = 2.250 \quad V_5 = \{v_5^1, v_5^2\} \quad \text{prio}_5 = 1 \quad \text{proc}_5 = 2$$

$$C_5^1 = 0.500 \quad \text{pd}_5^1 = 1.000 \quad \text{CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$$

$$C_5^2 = 0.125 \quad \text{pd}_5^2 = 0.500 \quad \text{CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$$

Carnegie Mellon University Software Engineering Institute Task 1

 $|\tau| = 5$ procs(Π) = { P_1, P_2 } $T_1 = 1.500 \quad D_1 = 1.500 \quad V_1 = \{v_1^1\} \quad \text{prio}_1 = 3 \quad \text{proc}_1 = 1$ = 0.250 pd_1^1 = 0.500 $\text{CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ C_1^1 $T_2 = 2.000 \quad D_2 = 2.000 \quad V_2 = \{v_2^1\} \quad \text{prio}_2 = 2 \quad \text{proc}_2 = 1$ Task 2 $= 0.250 \text{ pd}_2^1 = 0.500 \text{ CO}_2^1 = \{(\{v_2^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ C_2^1 $T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$ $C_{2}^{1} = 0.250 \text{ pd}_{3}^{1} = 0.500 \text{ CO}_{2}^{1} = \{(\{v_{1}^{1}\}, 1.0), (\{v_{2}^{1}\}, 0.5)\}$ $T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$ $C_4^1 = 0.250 \text{ pd}_4^1 = 0.500 \text{ CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$ $T_5 = 2.250$ $D_5 = 2.250$ $V_5 = \{v_5^1, v_5^2\}$ prio₅ = 1 proc₅ = 2 $C_5^1 = 0.500 \text{ pd}_5^1 = 1.000 \text{ CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$ $C_5^2 = 0.125 \text{ pd}_5^2 = 0.500 \text{ CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$

$ \tau = 5$	$\operatorname{procs}(\Pi) = \{P$	P_1, P_2 }	
		$\begin{split} V_1 &= \{v_1^1\} & \text{prio}_1 = 3 & \text{proc}_1 = 1 \\ \text{CO}_1^1 &= \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \end{split}$	
		$V_2 = \{v_2^1\} \text{prio}_2 = 2 \text{proc}_2 = 1$ $CO_2^1 = \{(\{v_3^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$	_
		$V_3 = \{v_3^1\} \text{prio}_3 = 3 \text{proc}_3 = 2$ $CO_3^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 0.5)\}$	Task 3
		$V_4 = \{v_4^1\} \text{prio}_4 = 2 \text{proc}_4 = 2$ $CO_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$	
$C_5^1 = 0.500$	$pd_5^1 = 1.000$	$V_{5} = \{v_{5}^{1}, v_{5}^{2}\} \text{ prio}_{5} = 1 \text{ proc}_{5} = 2$ $CO_{5}^{1} = \{(\{v_{1}^{1}\}, 1.0), (\{v_{2}^{1}\}, 1.0)\}$ $CO_{5}^{2} = \{(\{v_{1}^{1}\}, 0.5), (\{v_{2}^{1}\}, 1.0)\}$	

 $|\tau| = 5$ procs(Π) = { P_1, P_2 } $T_1 = 1.500 \quad D_1 = 1.500 \quad V_1 = \{v_1^1\} \quad \text{prio}_1 = 3 \quad \text{proc}_1 = 1$ = 0.250 pd_1^1 = 0.500 $\text{CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ C_1^1 $T_2 = 2.000 \quad D_2 = 2.000 \quad V_2 = \{v_2^1\} \quad \text{prio}_2 = 2 \quad \text{proc}_2 = 1$ $C_2^1 = 0.250 \text{ pd}_2^1 = 0.500 \text{ CO}_2^1 = \{(\{v_3\}, 0.5), (\{v_4\}, 1.0), (\{v_5\}, 1.0), (\{v_5\}, 1.0)\}$ $T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$ $C_{2}^{1} = 0.250 \text{ pd}_{3}^{1} = 0.500 \text{ CO}_{2}^{1} = \{(\{v_{1}^{1}\}, 1.0), (\{v_{2}^{1}\}, 0.5)\}$ $T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$ C^1_4 $= 0.250 \text{ pd}_4^1 = 0.500 \text{ CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$ $T_5 = 2.250$ $D_5 = 2.250$ $V_5 = \{v_5^1, v_5^2\}$ prio₅ = 1 proc₅ = 2 $C_5^1 = 0.500 \text{ pd}_5^1 = 1.000 \text{ CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$ $C_5^2 = 0.125 \text{ pd}_5^2 = 0.500 \text{ CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$

Carnegie Mellon University Software Engineering Institute Task 4

 $|\tau| = 5$ procs $(\Pi) = \{P_1, P_2\}$ $T_1 = 1.500 \quad D_1 = 1.500 \quad V_1 = \{v_1^1\} \quad \text{prio}_1 = 3 \quad \text{proc}_1 = 1$ $= 0.250 \text{ pd}_1^1 = 0.500 \text{ CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ C_1^1 $T_2 = 2.000 \quad D_2 = 2.000 \quad V_2 = \{v_2^1\} \quad \text{prio}_2 = 2 \quad \text{proc}_2 = 1$ $C_2^1 = 0.250 \text{ pd}_2^1 = 0.500 \text{ CO}_2^1 = \{(\{v_3\}, 0.5), (\{v_4\}, 1.0), (\{v_5\}, 1.0), (\{v_5\}, 1.0)\}$ $T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$ $C_{2}^{1} = 0.250 \text{ pd}_{3}^{1} = 0.500 \text{ CO}_{2}^{1} = \{(\{v_{1}^{1}\}, 1.0), (\{v_{2}^{1}\}, 0.5)\}$ $T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$ $C_4^1 = 0.250 \text{ pd}_4^1 = 0.500 \text{ CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$ $T_5 = 2.250$ $D_5 = 2.250$ $V_5 = \{v_5^1, v_5^2\}$ prio₅ = 1 proc₅ = 2 $C_5^1 = 0.500 \text{ pd}_5^1 = 1.000 \text{ CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$ $= 0.125 \text{ pd}_5^2 = 0.500 \text{ CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$ C_{5}^{2}

Task 5

Carnegie Mellon University Software Engineering Institute

$ \tau = 5$ $\operatorname{procs}(\Pi) = \{P_1, P_2\}$ Minimum inter-arrival times of tasks						
				$V_1 = \{v_1^1\} \\ CO_1^1 = \{(\{v_3^1\}, $		$proc_1 = 1$ 0.5), ({ v_5^1 }, 1.0), ({ v_5^2 }, 1.0)}
				$V_2 = \{v_2^1\}$ $CO_2^1 = \{(\{v_3^1\},$		$proc_2 = 1$ 1.0), ({ v_5^1 }, 1.0), ({ v_5^2 }, 1.0)}
				$V_3 = \{v_3^1\}$ $CO_3^1 = \{(\{v_1^1\},$	-	-
				$V_4 = \{v_4^1\}$ $CO_4^1 = \{(\{v_1^1\},$	-	-
C_5^1	= 0.500	pd_5^1	= 1.000	$V_5 = \{v_5^1, v_5^2\}$ $CO_5^1 = \{(\{v_1^1\}, CO_5^2) = \{(\{v_1^1\}, (v_1^1)\}, CO_5^2) = \{(\{v_1^1\}, (v_1^1)\}, (v_1^1)\}, (v_1^1) = \{(v_1^1)\}, (v_1^1)\}$	$(1.0), (\{v_2^1\},$	1.0)}

$$\begin{aligned} |\tau| &= 5 & \operatorname{procs}(\Pi) = \{P_1, P_2\} \\ & \begin{array}{r} \mathbf{Deadlines of} \\ \mathbf{Daadlines of} \\ \mathbf{tasks} \\ V_1 &= \{v_1^1\} & \operatorname{prio}_1 &= 3 & \operatorname{proc}_1 &= 1 \\ C_1^1 &= 0.250 & \operatorname{pd}_1^1 &= 0.500 & \operatorname{CO}_1^1 &= \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ T_2 &= 2.000 & \boxed{D_2 &= 2.000} & V_2 &= \{v_2^1\} & \operatorname{prio}_2 &= 2 & \operatorname{proc}_2 &= 1 \\ C_2^1 &= 0.250 & \operatorname{pd}_2^1 &= 0.500 & \operatorname{CO}_2^1 &= \{(\{v_3^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ T_3 &= 2.000 & \boxed{D_3 &= 2.000} & V_3 &= \{v_3^1\} & \operatorname{prio}_3 &= 3 & \operatorname{proc}_3 &= 2 \\ C_3^1 &= 0.250 & \operatorname{pd}_3^1 &= 0.500 & \operatorname{CO}_3^1 &= \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 0.5)\} \\ T_4 &= 2.000 & \boxed{D_4 &= 2.000} & V_4 &= \{v_4^1\} & \operatorname{prio}_4 &= 2 & \operatorname{proc}_4 &= 2 \\ C_4^1 &= 0.250 & \operatorname{pd}_4^1 &= 0.500 & \operatorname{CO}_4^1 &= \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\} \\ T_5 &= 2.250 & \boxed{D_5 &= 2.250} & V_5 &= \{v_5^1, v_5^2\} & \operatorname{prio}_5 &= 1 & \operatorname{proc}_5 &= 2 \\ C_5^1 &= 0.500 & \operatorname{pd}_5^1 &= 1.000 & \operatorname{CO}_5^1 &= \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\} \\ C_5^2 &= 0.125 & \operatorname{pd}_5^2 &= 0.500 & \operatorname{CO}_5^2 &= \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\} \\ \end{array}$$

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$$\begin{aligned} |\tau| &= 5 & \text{procs}(\Pi) = \{P_1, P_2\} \\ & \textbf{Sets of segments for each task} \\ T_1 &= 1.500 & D_1 &= 1.500 & V_1 = \{v_1^1\} & \text{prio}_1 = 3 & \text{proc}_1 = 1 \\ C_1^1 &= 0.250 & \text{pd}_1^1 &= 0.500 & \text{CO}_1^1 = \{(\{v_1^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ T_2 &= 2.000 & D_2 &= 2.000 & V_2 = \{v_2^1\} & \text{prio}_2 = 2 & \text{proc}_2 = 1 \\ C_2^1 &= 0.250 & \text{pd}_2^1 &= 0.500 & \text{CO}_2^1 = \{(\{v_1^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ T_3 &= 2.000 & D_3 &= 2.000 & V_3 = \{v_3^1\} & \text{prio}_3 = 3 & \text{proc}_3 = 2 \\ C_3^1 &= 0.250 & \text{pd}_3^1 &= 0.500 & \text{CO}_3^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 0.5)\} \\ T_4 &= 2.000 & D_4 &= 2.000 & V_4 = \{v_4^1\} & \text{prio}_4 = 2 & \text{proc}_4 = 2 \\ C_4^1 &= 0.250 & \text{pd}_4^1 &= 0.500 & \text{CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\} \\ T_5 &= 2.250 & D_5 &= 2.250 & V_5 = \{v_5^1, v_5^2\} & \text{prio}_5 = 1 & \text{proc}_5 = 2 \\ C_5^1 &= 0.500 & \text{pd}_5^1 &= 1.000 & \text{CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\} \\ C_5^2 &= 0.125 & \text{pd}_5^2 &= 0.500 & \text{CO}_2^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\} \\ \end{aligned}$$

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$$\begin{aligned} |\tau| &= 5 & \operatorname{procs}(\Pi) = \{P_1, P_2\} \\ T_1 &= 1.500 & D_1 &= 1.500 \underbrace{V_1 = \{v_1^1\}}_{1} & \operatorname{prio}_1 = 3 \quad \operatorname{proc}_1 = 1 & \operatorname{Task 1 has 1 segmen} \\ C_1^1 &= 0.250 & \operatorname{pd}_1^1 &= 0.500 & \operatorname{CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ T_2 &= 2.000 & D_2 &= 2.000 & V_2 = \{v_2^1\} & \operatorname{prio}_2 = 2 \quad \operatorname{proc}_2 = 1 \\ C_2^1 &= 0.250 & \operatorname{pd}_2^1 &= 0.500 & \operatorname{CO}_2^1 = \{(\{v_3^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ T_3 &= 2.000 & D_3 &= 2.000 & V_3 = \{v_3^1\} & \operatorname{prio}_3 = 3 \quad \operatorname{proc}_3 = 2 \\ C_3^1 &= 0.250 & \operatorname{pd}_3^1 &= 0.500 & \operatorname{CO}_3^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 0.5)\} \\ T_4 &= 2.000 & D_4 &= 2.000 & V_4 = \{v_4^1\} & \operatorname{prio}_4 = 2 \quad \operatorname{proc}_4 = 2 \\ C_4^1 &= 0.250 & \operatorname{pd}_4^1 &= 0.500 & \operatorname{CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\} \\ T_5 &= 2.250 & D_5 &= 2.250 & V_5 = \{v_5^1, v_5^2\} & \operatorname{prio}_5 = 1 \quad \operatorname{proc}_5 = 2 \\ C_5^1 &= 0.500 & \operatorname{pd}_5^1 &= 1.000 & \operatorname{CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\} \\ C_5^2 &= 0.125 & \operatorname{pd}_5^2 &= 0.500 & \operatorname{CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\} \\ \end{aligned}$$

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 $|\tau| = 5$ procs $(\Pi) = \{P_1, P_2\}$ $T_1 = 1.500 \quad D_1 = 1.500 \quad V_1 = \{v_1^1\} \quad \text{prio}_1 = 3 \quad \text{proc}_1 = 1$ = 0.250 pd_1^1 = 0.500 $\text{CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ C_1^1 $T_2 = 2.000 \quad D_2 = 2.000 \quad V_2 = \{v_2^1\} \quad \text{prio}_2 = 2 \quad \text{proc}_2 = 1$ $C_2^1 = 0.250 \text{ pd}_2^1 = 0.500 \text{ CO}_2^1 = \{(\{v_3\}, 0.5), (\{v_4\}, 1.0), (\{v_5\}, 1.0), (\{v_5\}, 1.0)\}$ $T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$ $C_{2}^{1} = 0.250 \text{ pd}_{3}^{1} = 0.500 \text{ CO}_{2}^{1} = \{(\{v_{1}^{1}\}, 1.0), (\{v_{2}^{1}\}, 0.5)\}$ $T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$ $C_4^1 = 0.250 \text{ pd}_4^1 = 0.500 \text{ CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$ $T_5 = 2.250$ $D_5 = 2.250$ $V_5 = \{v_5^1, v_5^2\}$ prio₅ = 1 proc₅ = 2 $C_5^1 = 0.500 \text{ pd}_5^1 = 1.000 \text{ CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$ $C_5^2 = 0.125 \text{ pd}_5^2 = 0.500 \text{ CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$

Carnegie Mellon University Software Engineering Institute Task 5 has 2 segments.

$$\begin{aligned} |\tau| &= 5 & \operatorname{procs}(\Pi) = \{P_1, P_2\} \\ \hline \mathbf{Priorities for each task} \\ T_1 &= 1.500 & D_1 &= 1.500 & V_1 = \{v_1^1\} & \underline{\operatorname{prio}_1 = 3} & \operatorname{proc}_1 = 1 \\ C_1^1 &= 0.250 & \mathrm{pd}_1^1 &= 0.500 & \mathrm{CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ T_2 &= 2.000 & D_2 &= 2.000 & V_2 = \{v_2^1\} & \underline{\operatorname{prio}_2 = 2} & \operatorname{proc}_2 = 1 \\ C_2^1 &= 0.250 & \mathrm{pd}_2^1 &= 0.500 & \mathrm{CO}_2^1 = \{(\{v_3^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ T_3 &= 2.000 & D_3 &= 2.000 & V_3 = \{v_3^1\} & \underline{\operatorname{prio}_3 = 3} & \operatorname{proc}_3 = 2 \\ C_3^1 &= 0.250 & \mathrm{pd}_3^1 &= 0.500 & \mathrm{CO}_3^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 0.5)\} \\ T_4 &= 2.000 & D_4 &= 2.000 & V_4 = \{v_4^1\} & \underline{\operatorname{prio}_4 = 2} & \mathrm{proc}_4 = 2 \\ C_4^1 &= 0.250 & \mathrm{pd}_4^1 &= 0.500 & \mathrm{CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\} \\ T_5 &= 2.250 & D_5 &= 2.250 & V_5 = \{v_5^1, v_5^2\} & \underline{\operatorname{prio}_5 = 1} & \mathrm{proc}_5 = 2 \\ C_5^1 &= 0.500 & \mathrm{pd}_5^1 &= 1.000 & \mathrm{CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\} \\ C_5^2 &= 0.125 & \mathrm{pd}_5^2 &= 0.500 & \mathrm{CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\} \\ \hline \end{aligned}$$

 $|\tau| = 5$ procs $(\Pi) = \{P_1, P_2\}$ Processor to each task is assigned $T_1 = 1.500 \quad D_1 = 1.500 \quad V_1 = \{v_1^1\} \quad \text{prio}_1 = 3 \quad \text{proc}_1 = 1$ $= 0.250 \text{ pd}_1^1 = 0.500 \text{ CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ C^1 $T_2 = 2.000 \quad D_2 = 2.000 \quad V_2 = \{v_2^1\} \quad \text{prio}_2 = 2 \quad \text{proc}_2 = 1$ $C_2^1 = 0.250 \text{ pd}_2^1 = 0.500 \text{ CO}_2^1 = \{(\{v_2^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ $T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$ $C_{2}^{1} = 0.250 \text{ pd}_{3}^{1} = 0.500 \text{ CO}_{2}^{1} = \{(\{v_{1}^{1}\}, 1.0), (\{v_{2}^{1}\}, 0.5)\}$ $T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$ $C_4^1 = 0.250 \text{ pd}_4^1 = 0.500 \text{ CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$ $T_5 = 2.250 \quad D_5 = 2.250 \quad V_5 = \{v_5^1, v_5^2\} \quad \text{prio}_5 = 1 \quad \text{proc}_5 = 2$ $C_5^1 = 0.500 \text{ pd}_5^1 = 1.000 \text{ CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$ $C_5^2 = 0.125 \text{ pd}_5^2 = 0.500 \text{ CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$

 $\begin{array}{ll} |\tau| = 5 & \operatorname{procs}(\Pi) = \{P_1, P_2\} \\ \hline \mathbf{Execution \ requirement \ for \ each \ segment \ of \ each \ task} \\ T_1 &= 1.500 & D_1 &= 1.500 & V_1 = \{v_1^1\} & \operatorname{prio}_1 = 3 & \operatorname{proc}_1 = 1 \\ \hline C_1^1 &= 0.250 & \operatorname{pd}_1^1 &= 0.500 & \operatorname{CO}_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \end{array}$

$$\begin{array}{cccc} T_3 &= 2.000 & D_3 &= 2.000 & V_3 = \{v_3^1\} & \text{prio}_3 = 3 & \text{proc}_3 = 2\\ \hline C_3^1 &= 0.250 & \text{pd}_3^1 &= 0.500 & \text{CO}_3^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 0.5)\} \end{array}$$

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$$\begin{aligned} |\tau| &= 5 & \operatorname{procs}(\Pi) = \{P_1, P_2\} \\ & \begin{array}{c} & \begin{array}{c} \text{Speed as function of co-runners} \\ & V_1 = \{v_1^1\} & \operatorname{prio}_1 = 3 & \operatorname{proc}_1 = 1 \\ \hline C_1^1 &= 0.250 & \operatorname{pd}_1^1 &= 0.500 \\ \hline C_1^1 &= \{(\{v_1^1\}, 1.0), (\{v_1^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ \hline \\ & T_2 &= 2.000 & D_2 &= 2.000 \\ \hline C_2^1 &= 0.250 & \operatorname{pd}_2^1 &= 0.500 \\ \hline C_2^1 &= \{(\{v_1^1\}, 0.5), (\{v_1^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ \hline \\ & T_3 &= 2.000 & D_3 &= 2.000 \\ \hline C_2^1 &= \{(\{v_1^1\}, 1.0), (\{v_1^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\} \\ \hline \\ & T_3 &= 2.000 & D_3 &= 2.000 \\ \hline \\ & C_3^1 &= 0.250 & \operatorname{pd}_3^1 &= 0.500 \\ \hline \\ & C_3^1 &= 0.250 & \operatorname{pd}_3^1 &= 0.500 \\ \hline \\ & C_4^1 &= 0.250 & \operatorname{pd}_4^1 &= 0.500 \\ \hline \\ & C_4^1 &= 0.250 & \operatorname{pd}_4^1 &= 0.500 \\ \hline \\ & C_5 &= 0.125 & \operatorname{pd}_5^2 &= 1.000 \\ \hline \\ & C_5^2 &= 0.125 & \operatorname{pd}_5^2 &= 0.500 \\ \hline \\ & C_5 &= 0.125 & \operatorname{pd}_5^2 &= 0.500 \\ \hline \\ & C_5 &= 0.125 & \operatorname{pd}_5^2 &= 0.500 \\ \hline \end{array}$$

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SBESC 2019 Taskset example

If segment 1 of task 1 executes in parallel with segment 1 of task 4, $|\tau| = 5$ procs $(\Pi) = \{P_1, P_2\}$ then Segment 1 of task 1 executes with speed 0.5. $T_1 = 1.500 \quad D_1 = 1.500 \quad V_1 = \{v_1^1\} \quad \text{prio}_1 = 3 \quad \text{proc}_1 = 1$ $C_1^1 = 0.250 \quad \mathrm{pd}_1^1 = 0.500 \quad \mathrm{CO}_1^1 = \{(\{v_3^1\}, 1.0), \overline{(\{v_4^1\}, 0.5)}, (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ $T_2 = 2.000 \quad D_2 = 2.000 \quad V_2 = \{v_2^1\} \quad \text{prio}_2 = 2 \quad \text{proc}_2 = 1$ $C_2^1 = 0.250 \text{ pd}_2^1 = 0.500 \text{ CO}_2^1 = \{(\{v_2^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$ $T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$ $C_2^1 = 0.250 \text{ pd}_3^1 = 0.500 \text{ CO}_3^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 0.5)\}$ $T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$ $C_4^1 = 0.250 \text{ pd}_4^1 = 0.500 \text{ CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$ $T_5 = 2.250$ $D_5 = 2.250$ $V_5 = \{v_5^1, v_5^2\}$ prio₅ = 1 proc₅ = 2 $C_5^1 = 0.500 \text{ pd}_5^1 = 1.000 \text{ CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$ $C_5^2 = 0.125 \text{ pd}_5^2 = 0.500 \text{ CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$

SBESC 2019 Taskset example

 $|\tau| = 5$

nple If segment 1 of task 1 executes in parallel with a segmentset for which information in CO is not available, then segment 1 of task 1 $\operatorname{procs}(\Pi) = \{P_1, P_2\}$ executes with speed 0.5.

$$T_1 = 1.500 \quad D_1 = 1.500 \quad V_1 = \{v_1^1\} \quad \text{prio}_1 = 3 \quad \text{proc}_1 = 1$$

$$C_1^1 = 0.250 \quad \boxed{\text{pd}_1^1 = 0.500} \quad CO_1^1 = \{(\{v_3^1\}, 1.0), (\{v_4^1\}, 0.5), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$$

$$T_2 = 2.000 \quad D_2 = 2.000 \quad V_2 = \{v_2^1\} \quad \text{prio}_2 = 2 \quad \text{proc}_2 = 1$$

$$C_2^1 = 0.250 \quad \text{pd}_2^1 = 0.500 \quad \text{CO}_2^1 = \{(\{v_3^1\}, 0.5), (\{v_4^1\}, 1.0), (\{v_5^1\}, 1.0), (\{v_5^2\}, 1.0)\}$$

$$T_3 = 2.000 \quad D_3 = 2.000 \quad V_3 = \{v_3^1\} \quad \text{prio}_3 = 3 \quad \text{proc}_3 = 2$$

$$C_3^1 = 0.250 \quad \text{pd}_3^1 = 0.500 \quad \text{CO}_3^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 0.5)\}$$

$$T_4 = 2.000 \quad D_4 = 2.000 \quad V_4 = \{v_4^1\} \quad \text{prio}_4 = 2 \quad \text{proc}_4 = 2$$

$$C_4^1 = 0.250 \quad \text{pd}_4^1 = 0.500 \quad \text{CO}_4^1 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$$

$$T_5 = 2.250 \quad D_5 = 2.250 \quad V_5 = \{v_5^1, v_5^2\} \quad \text{prio}_5 = 1 \quad \text{proc}_5 = 2$$

$$C_5^1 = 0.500 \quad \text{pd}_5^1 = 1.000 \quad \text{CO}_5^1 = \{(\{v_1^1\}, 1.0), (\{v_2^1\}, 1.0)\}$$

$$C_5^2 = 0.125 \quad \text{pd}_5^2 = 0.500 \quad \text{CO}_5^2 = \{(\{v_1^1\}, 0.5), (\{v_2^1\}, 1.0)\}$$

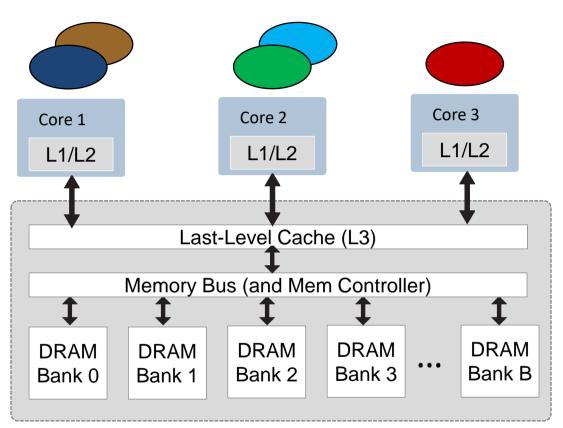
Big Research Questions

Q1: What is a good abstraction that describes the effect of undocumented hardware? (DONE)

Q2: How to create a schedulability analysis that uses this abstraction?

Before discussing them, let us discuss:

- 1. Other approaches (DONE)
- 2. General ideas for abstractions in other disciplines (DONE)

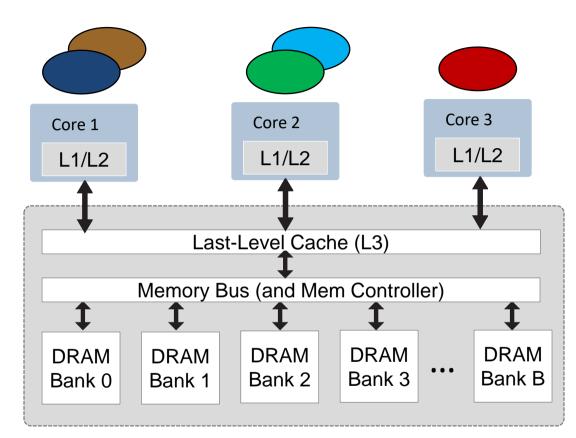


Big Research Questions

Q1: What is a good abstraction that describes the effect of undocumented hardware?

Q2: How to create a schedulability analysis that uses this abstraction?

Let us discuss Q2.

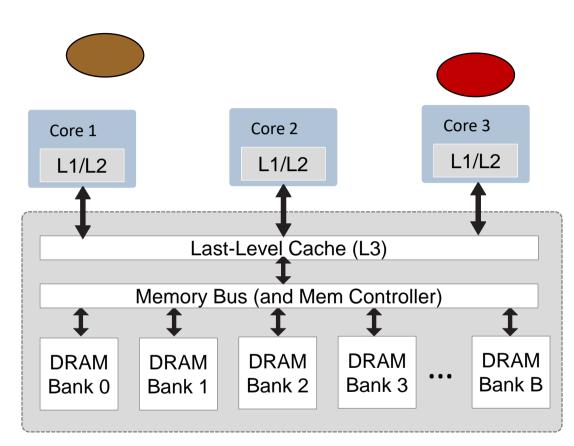


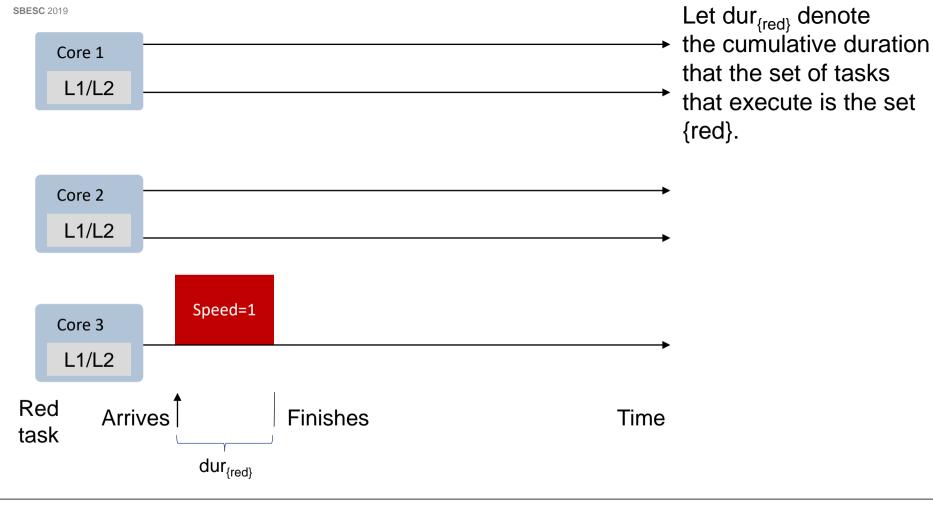
Big Research Questions

Q1: What is a good abstraction that describes the effect of undocumented hardware?

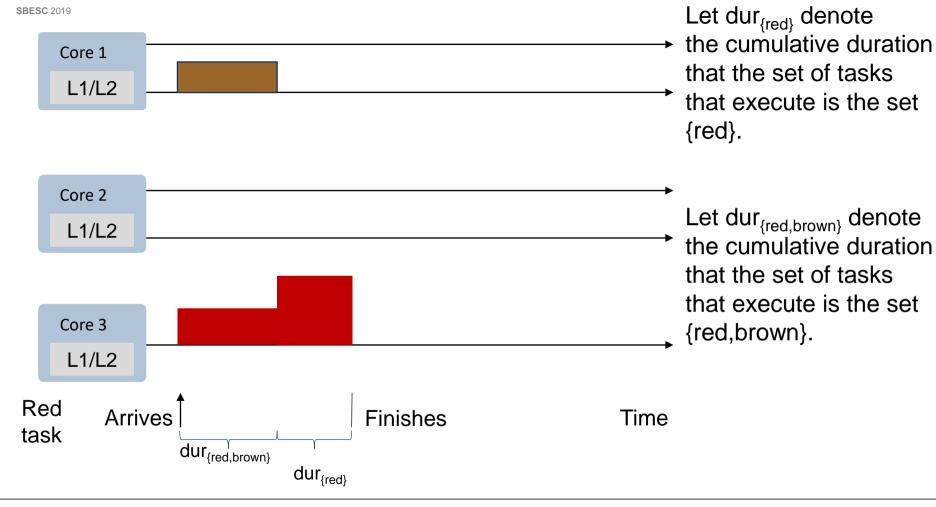
Q2: How to create a schedulability analysis that uses this abstraction?

In order to simplify our discussion initially, let us consider a taskset with only Red and Brown task. Also, let us consider that the minimum inter-arrival time of each of these tasks is infinity (i.e., generates just a single job).

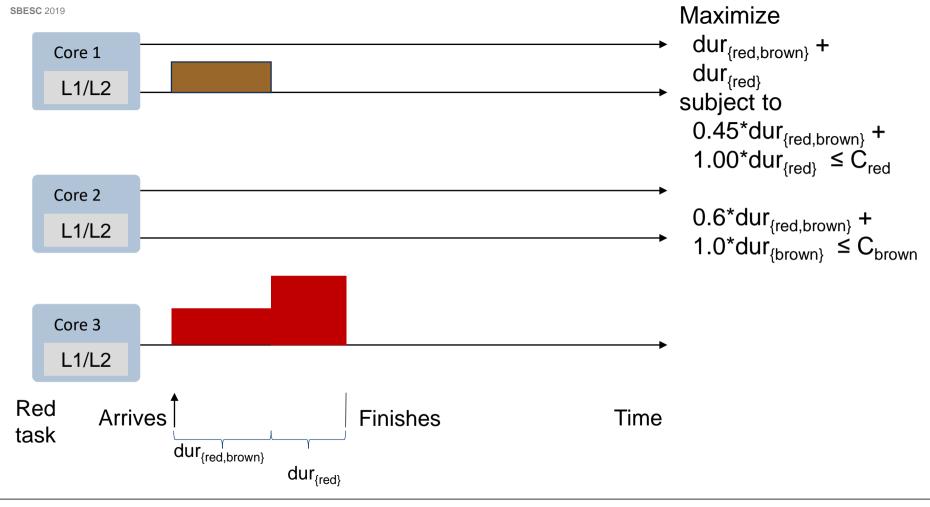




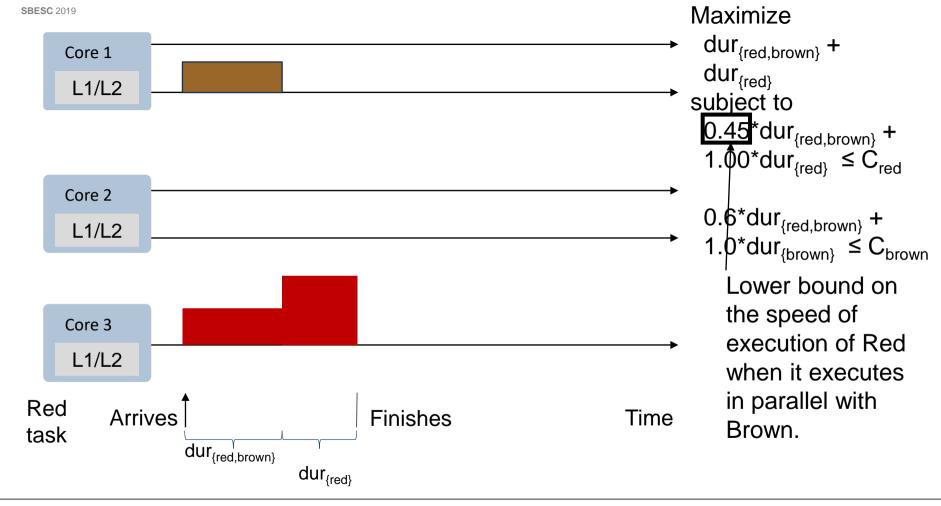
Timing Analysis of Software Executing on Undocumented Multicore Processors © 2019 Carnegie Mellon University

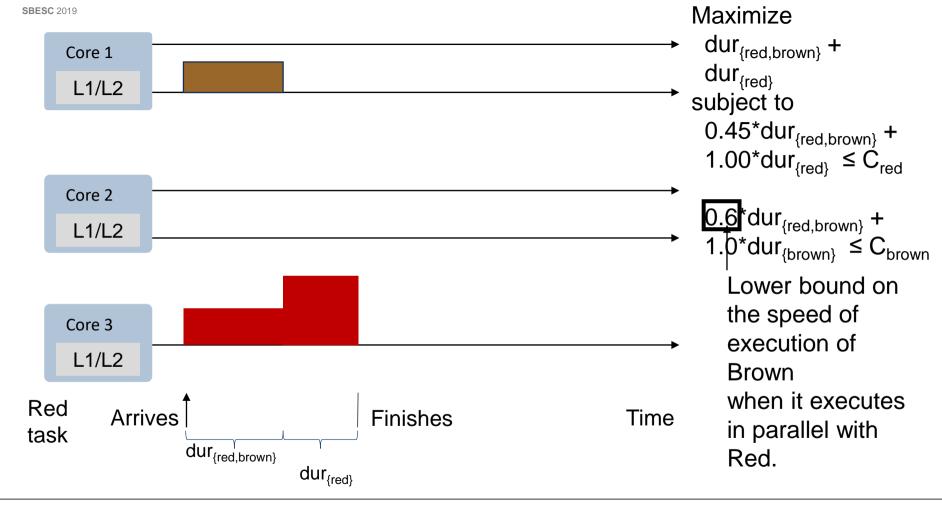


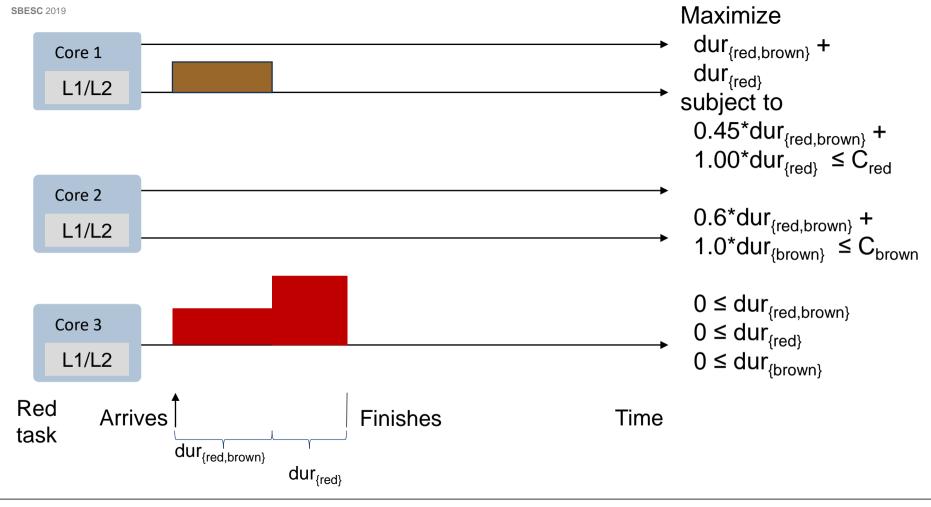
Timing Analysis of Software Executing on Undocumented Multicore Processors © 2019 Carnegie Mellon University

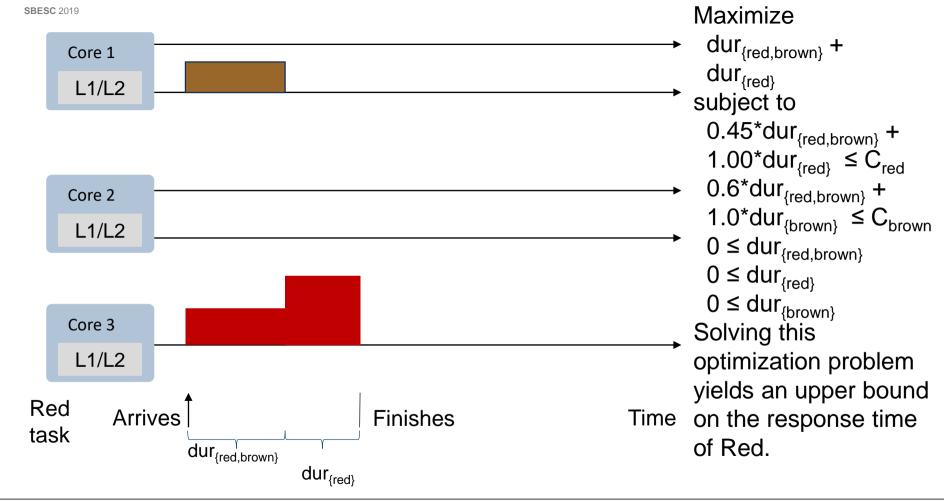


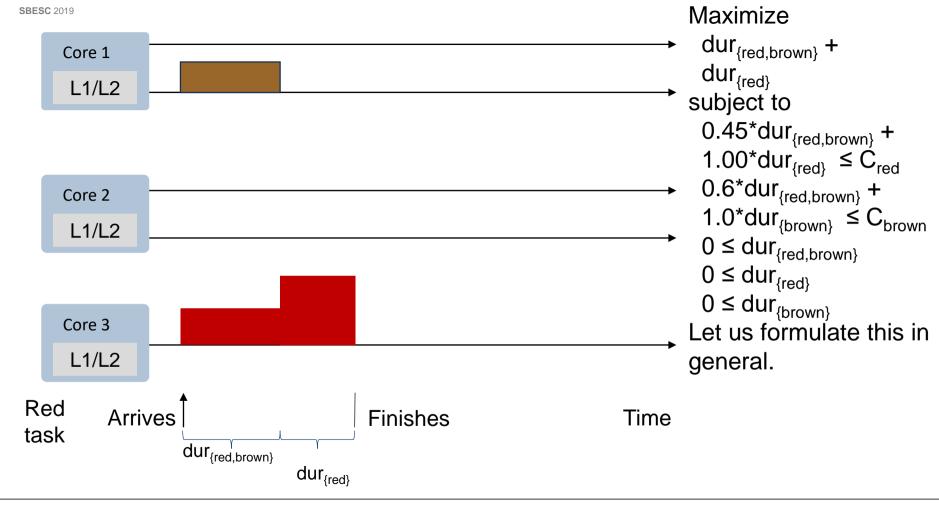
Timing Analysis of Software Executing on Undocumented Multicore Processors © 2019 Carnegie Mellon University

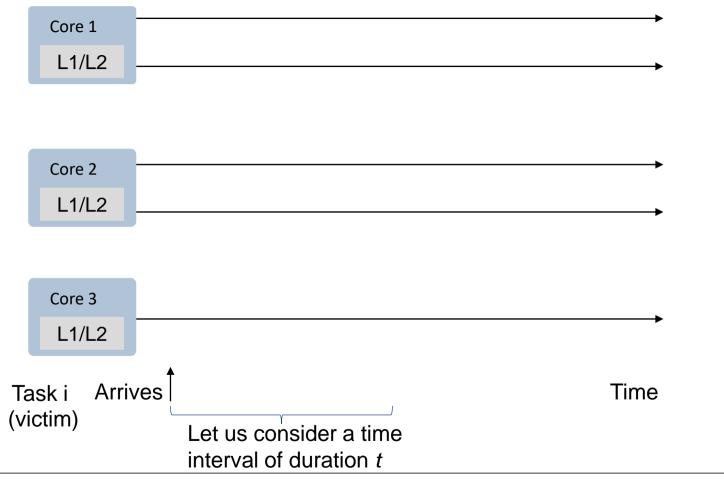


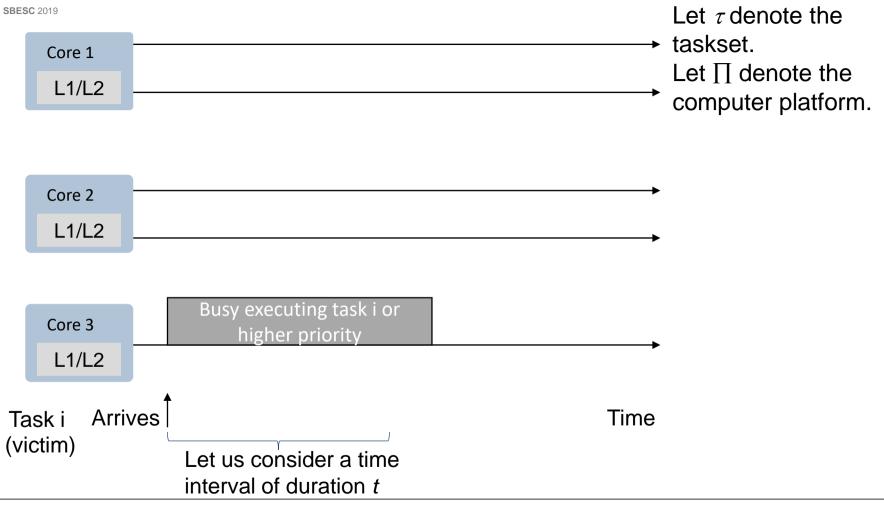


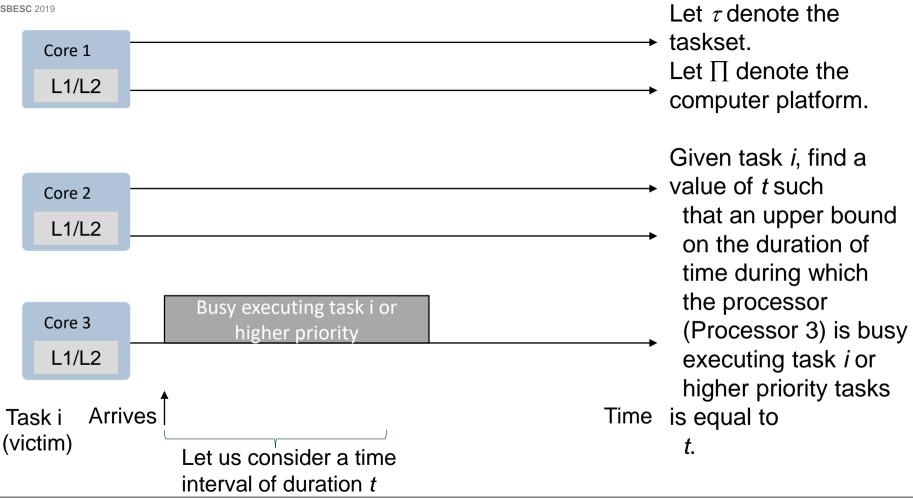


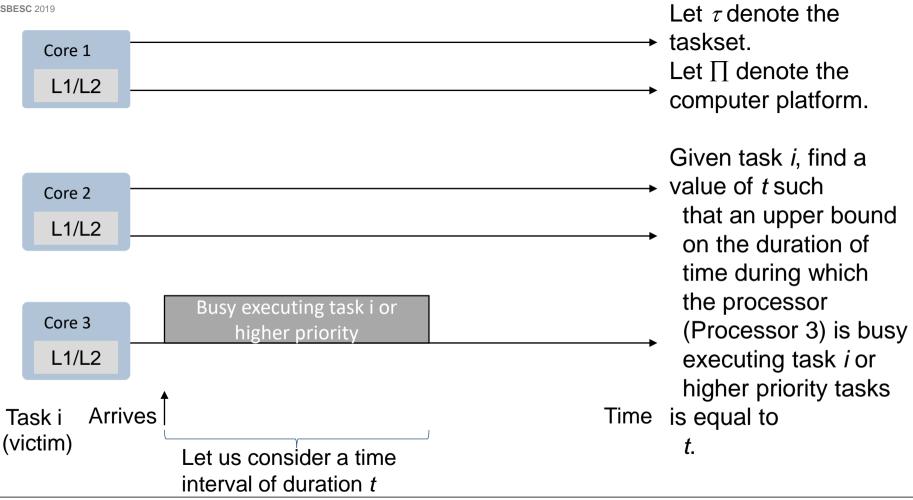












Define reqlp(τ , Π ,*i*,*t*) as the optimal value of the objective function of the following:

 \max imize

$$\sum_{i' \in \operatorname{hep}(\tau,\Pi,i)} \sum_{v_{i'}^{k'} \in V_{i'}} \sum_{s \in S(\tau,\Pi,i',k')} \operatorname{du}_s$$

subject to

$$\begin{aligned} \forall i' \in \operatorname{hep}(\tau, \Pi, i), \forall v_{i'}^{k'} \in V_{i'}, \sum_{s \in S(\tau, \Pi, i', k')} \operatorname{pw}_{i', s \setminus \{\langle i', k' \rangle\}}^{k'} \times \operatorname{du}_{s} &\leq \lceil \frac{t}{T_{i'}} \rceil \times C_{i'}^{k'} \\ \forall i' \in \operatorname{top}(\tau, \Pi, i), \forall v_{i'}^{k'} \in V_{i'}, \sum_{\substack{s \in S(\tau, \Pi, i', k') \land \\ (\exists \langle i'', k'' \rangle \text{ s.t. } (i'' \in \operatorname{hep}(\tau, \Pi, i)) \land (\langle i'', k'' \rangle \in s))} \\ \forall s \in S(\tau, \Pi) \text{ s.t. } (\exists \langle i'', k'' \rangle \text{ s.t. } (i'' \in \operatorname{hep}(\tau, \Pi, i)) \land (\langle i'', k'' \rangle \in s)), \operatorname{du}_{s} \in \mathbb{R}_{\geq 0} \end{aligned}$$

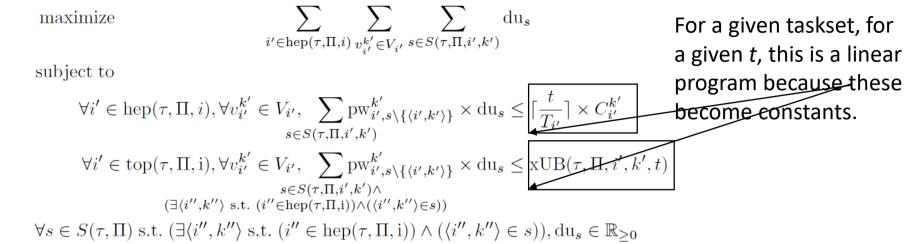
Schedulability analysis (timing verification) is done as follows:

THEOREM 4.2. $(\forall \tau_i \in \tau, (\exists t \in [0, D_i], \operatorname{reqlp}(\tau, \Pi, i, t) \leq t)) \Rightarrow \tau \text{ is schedulable on } \Pi$

Define reqlp(τ , Π ,*i*,*t*) as the optimal value of the objective function of the following:

THEOREM 4.2. $(\forall \tau_i \in \tau, (\exists t \in [0, D_i], \operatorname{reqlp}(\tau, \Pi, i, t) \leq t)) \Rightarrow \tau$ is schedulable on Π

Define reqlp(τ , Π ,*i*,*t*) as the optimal value of the objective function of the following:



Schedulability analysis (timing verification) is done as follows:

THEOREM 4.2. $(\forall \tau_i \in \tau, (\exists t \in [0, D_i], \operatorname{reqlp}(\tau, \Pi, i, t) \leq t)) \Rightarrow \tau \text{ is schedulable on } \Pi$

Define reqlp(τ , Π ,*i*,*t*) as the optimal value of the objective function of the following:

$$\begin{array}{ll} \text{maximize} & \sum_{i' \in \text{hep}(\tau,\Pi,i)} \sum_{v_{i'}^{k'} \in V_{i'}} \sum_{s \in S(\tau,\Pi,i',k')} \text{d}\mathbf{u}_{s} \\ \text{subject to} \\ & \forall i' \in \text{hep}(\tau,\Pi,i), \forall v_{i'}^{k'} \in V_{i'}, \sum_{s \in S(\tau,\Pi,i',k')} \text{pw}_{i',s \setminus \{\langle i',k' \rangle\}}^{k'} \times \text{d}\mathbf{u}_{s} \leq \lceil \frac{t}{T_{i'}} \rceil \times C_{i'}^{k'} \\ & \forall i' \in \text{top}(\tau,\Pi,i), \forall v_{i'}^{k'} \in V_{i'}, \sum_{s \in S(\tau,\Pi,i',k')} \text{pw}_{i',s \setminus \{\langle i',k' \rangle\}}^{k'} \times \text{d}\mathbf{u}_{s} \leq \text{xUB}(\tau,\Pi,i',k',t) \\ & \forall i' \in \text{top}(\tau,\Pi,i), \forall v_{i'}^{k'} \in V_{i'}, \sum_{s \in S(\tau,\Pi,i',k')} \text{pw}_{i',s \setminus \{\langle i',k' \rangle\}}^{k'} \times \text{d}\mathbf{u}_{s} \leq \text{xUB}(\tau,\Pi,i',k',t) \\ & \quad (\exists \langle i'',k'' \rangle \text{ s.t. } (i'' \in \text{hep}(\tau,\Pi,i)) \land (\langle i'',k'' \rangle \in s)) \\ \forall s \in S(\tau,\Pi) \text{ s.t. } (\exists \langle i'',k'' \rangle \text{ s.t. } (i'' \in \text{hep}(\tau,\Pi,i)) \land (\langle i'',k'' \rangle \in s)), \text{d}\mathbf{u}_{s} \in \mathbb{R}_{\geq 0} \end{array}$$

Schedulability analysis (timing verification) is done as follows:

THEOREM 4.2. $(\forall \tau_i \in \tau, (\exists t \in [0, D_i], \operatorname{reqlp}(\tau, \Pi, i, t) \leq t)) \Rightarrow \tau \text{ is schedulable on } \Pi$

Define reglp (τ, Π, i, t) as the optimal value of the objective function of the following:

$$\begin{array}{ll} \text{maximize} & \sum_{i' \in \text{hep}(\tau,\Pi,i)} \sum_{v_{i'}^{k'} \in V_{i'}} \sum_{s \in S(\tau,\Pi,i',k')} \text{d} u_s \\ \text{subject to} \\ & \forall i' \in \text{hep}(\tau,\Pi,i), \forall v_{i'}^{k'} \in V_{i'}, \sum_{s \in S(\tau,\Pi,i',k')} \text{pw}_{i',s \setminus \{\langle i',k' \rangle\}}^{k'} \times \text{d} u_s \leq \left\lceil \frac{t}{T_{i'}} \right\rceil \times C_{i'}^{k'} \\ & \forall i' \in \text{top}(\tau,\Pi,i), \forall v_{i'}^{k'} \in V_{i'}, \sum_{s \in S(\tau,\Pi,i',k')} \text{pw}_{i',s \setminus \{\langle i',k' \rangle\}}^{k'} \times \text{d} u_s \leq \text{xUB}(\tau,\Pi,i',k',t) \\ & \forall i' \in \text{top}(\tau,\Pi,i), \forall v_{i'}^{k'} \in V_{i'}, \sum_{s \in S(\tau,\Pi,i',k')} \text{pw}_{i',s \setminus \{\langle i',k' \rangle\}}^{k'} \times \text{d} u_s \leq \text{xUB}(\tau,\Pi,i',k',t) \\ & (\exists \langle i'',k'' \rangle \text{ s.t. } (i'' \in \text{hep}(\tau,\Pi,i)) \land (\langle i'',k'' \rangle \in s)) \\ \forall s \in S(\tau,\Pi) \text{ s.t. } (\exists \langle i'',k'' \rangle \text{ s.t. } (i'' \in \text{hep}(\tau,\Pi,i)) \land (\langle i'',k'' \rangle \in s)), \text{d} u_s \in \mathbb{R}_{\geq 0} \end{array}$$

Schedulability analysis (timing verification) is done as follows:

THEOREM 4.2. $(\forall \tau_i \in \tau, (\exists t \in [0, D_i], \operatorname{reqlp}(\tau, \Pi, i, t) \leq t)) \Rightarrow \tau$ is schedulable on Π

be done in

Define reqlp(τ , Π ,*i*,*t*) as the optimal value of the objective function of the following:

maximize

$$\sum_{i' \in \operatorname{hep}(\tau,\Pi,i)} \sum_{v_{i'}^{k'} \in V_{i'}} \sum_{s \in S(\tau,\Pi,i',k')} \operatorname{du}_s$$

subject to

$$\begin{aligned} \forall i' \in \operatorname{hep}(\tau, \Pi, i), \forall v_{i'}^{k'} \in V_{i'}, \sum_{s \in S(\tau, \Pi, i', k')} \operatorname{pw}_{i', s \setminus \{\langle i', k' \rangle\}}^{k'} \times \operatorname{du}_{s} &\leq \lceil \frac{t}{T_{i'}} \rceil \times C_{i'}^{k'} \\ \forall i' \in \operatorname{top}(\tau, \Pi, i), \forall v_{i'}^{k'} \in V_{i'}, \sum_{\substack{s \in S(\tau, \Pi, i', k') \land \\ (\exists \langle i'', k'' \rangle \text{ s.t. } (i'' \in \operatorname{hep}(\tau, \Pi, i)) \land (\langle i'', k'' \rangle \in s))} \\ \forall s \in S(\tau, \Pi) \text{ s.t. } (\exists \langle i'', k'' \rangle \text{ s.t. } (i'' \in \operatorname{hep}(\tau, \Pi, i)) \land (\langle i'', k'' \rangle \in s)), \operatorname{du}_{s} \in \mathbb{R}_{\geq 0} \end{aligned}$$

Schedulability analysis (timing verification) is done as follows:

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Define reqlp(τ , Π ,*i*,*t*) as the optimal value of the objective function of the following:

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 $\forall s$

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This is a generalization of the classic response-time analysis for Rate-Monotonic.

Define reqlp(τ , Π ,*i*,*t*) as the optimal value of the objective function of the following:

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subject to

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For details (about this theorem and other results about the model), see B. Andersson et al., ``Schedulability Analysis of Tasks with Co-Runner-Dependent Execution Times,'' ACM TECS, 2018.

Define reqlp(τ , Π ,*i*,*t*) as the optimal value of the objective function of the following:

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Schedulability analysis (timing verification) is done as follows:

THEOREM 4.2. $(\forall \tau_i \in \tau, (\exists t \in [0, D_i], \operatorname{reqlp}(\tau, \Pi, i, t) \leq t)) \Rightarrow \tau \text{ is schedulable on } \Pi$

We have a schedulability analysis for tasks with co-runner dependent execution times.

Comparing this result to classic Rate-Monotonic Analysis

Work	Model	Time Complexity	Formulation	Time Complexity
	(Execution	of Exact	of Schedulability	of Schedulability
	Time Depends	Schedulability	Test	Test
	on Corunners)	Analysis		
Previous	No	\leq Pseudo-	$(\forall \tau_i \in \tau, (\exists t \in [0, D_i],$	Pseudo-polynomial
work		polynomial	$\sum_{j \in \operatorname{hep}(\tau,\Pi,i)} \left\lceil \frac{t}{T_j} \right\rceil C_j \le t))$	
			\Leftrightarrow schedulable	
This	Yes	Co-NP-hard	$(\forall \tau_i \in \tau, (\exists t \in [0, D_i],$	Pseudo-polynomial
article		in the strong	$\operatorname{reqlp}(\tau,\Pi,i,t) \leq t))$	if the number of
		sense	\Rightarrow schedulable	processors in Π
				is fixed

This result generalizes classic Rate-Monotonic Analysis to undocumented multicore

Work	Model	Time Complexity	Formulation	Time Complexity
	(Execution	of Exact	of Schedulability	of Schedulability
	Time Depends	Schedulability	Test	Test
	on Corunners)	Analysis		
Previous	No	\leq Pseudo-	$(\forall \tau_i \in \tau, (\exists t \in [0, D_i],$	Pseudo-polynomial
work		polynomial	$\sum_{j \in \operatorname{hep}(\tau,\Pi,i)} \left\lceil \frac{t}{T_j} \right\rceil C_j \le t))$	
			\Leftrightarrow schedulable	
This	Yes	Co-NP-hard	$(\forall \tau_i \in \tau, (\exists t \in [0, D_i],$	Pseudo-polynomial
article		in the strong	$\operatorname{reqlp}(\tau,\Pi,i,t) \leq t))$	if the number of
		sense	\Rightarrow schedulable	processors in Π
				is fixed

This looks very theoretical. Does this really work in reality?



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I understand that for each task, the set of corunner sets is polynomial in the number of tasks assuming that the number of processors is fixed.

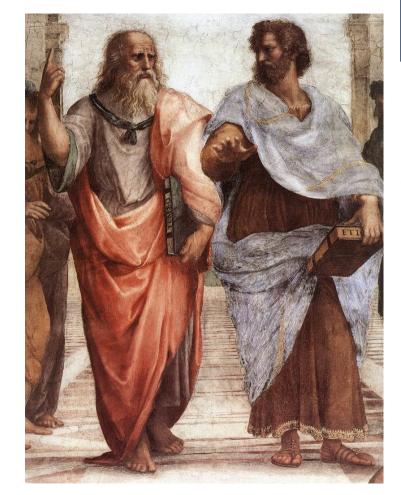


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But I still wonder how one can obtain the lower bound of speed of execution of one task given co-runners.



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A measurement-based approach:

5.2 Obtaining Taskset Parameters for a Given Software System

Every scheduling theory that provides 100% guarantees on timing relies on a model. Traditional scheduling theory relies on knowledge of an upper bound on the execution time of a program, and therefore, the research community has developed methods for finding an upper bound on the execution requirement of a program when the program runs in isolation on a single-core processor (Wilhelm et al. 2008). One can distinguish between (1) *static methods* that take the program as input and compute an upper bound without running the program. (2) *hybrid methods* that measure execution times of parts of a program and then use static methods to compute an upper bound for the entire program, and (3) *dynamic methods* where a software practitioner uses domain knowledge to identify a set of worst-case inputs/initial states of the program and then measures the execution time of the program for these inputs/initial states (5) sometimes the program is run multiple times with variations of inputs/initial state and sometimes a safety margin is added based on engineering judgment. The dynamic method is in common use in industry today.

The model used in this article, however, also requires that a task/segment is described with a lower bound on its speed as a function of corunners. Unfortunately, the current state of the art does not offer any method for obtaining such a lower bound while considering all the complexities of modern memory systems. Therefore, in order to use our scheduling theory (in practice and also in our case study/validation in Section 5.3), we need to develop a method for obtaining such a lower bound. We will do so by using method (3) mentioned above but extending it so that it also provides a lower bound on its speed as a function of corunners. The new method is shown below as pseudo-code:

- Let SS be an integer indicating the sample size used in our experimental method. Assign a value to SS (for example SS := 100).
- (2) For each task τ_i ∈ τ, for each v^k_i ∈ V_i, do
- (a) Run a job of task τ_i on the computer platform s.t. no other tasks execute on this platform.
- (b) Repeat the measurement SS times and let CMI^k₁ denote the set of these measurements (execution times from measurements of a task executed in isolation).
- (3) For each task $\tau_i \in \tau$, for each $v_i^k \in V_i$, do $C_i^k := \max_{x \in CMI_i^k} x$.
- (4) For each task τ_i ∈ τ, for each v^k_i ∈ V_i, do
 - (a) Find an upper bound on the number of memory accesses performed by a segment of a job of task r_i. (This can be obtained using performance monitoring counters.) Run these measurements SS times. Let H^k_i denote the largest measurement.
 - (b) Find an upper bound on the time for a single <u>memory access assuming that we do not</u> know the corunners. Let MA denote this (e.g., MA could be 500 nanoseconds).
- (c) $pd_i^k := \max_{x \in CMI_i^k} \frac{x}{x + H_i^k \times MA}$.
- (5) For each task τ_i ∈ τ, for each v^k_i ∈ V_i, do CO^k_i := Ø.
- (6) For each task τ_i ∈ τ, for each v^k_i ∈ V_i, for each s ∈ S(τ, Π, i, k), do
- (a) co := $s \setminus \{\langle i, k \rangle\}$.
- (b) For those segments in co, keep running all of them continuously (i.e., if segment v^F_ρ is in no, then when v^F_ρ has finished execution, let this segment v^F_ρ start execution again immediately).
- (c) While the segments in (b) execute continuously, execute a single job of segment v^k_i of task r_i and measure the execution time of v^k_i. Repeat this measurement SS times and let CMC^k_{kco} denote the set of measurements (exe<u>c</u>ution times from <u>measurements</u> of a task executed with <u>co-runners</u>).

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OK, I buy that you can obtain these lower bounds on the speed of execution through measurements. But I wonder how trustworthy these numbers are. Have you done any validation?



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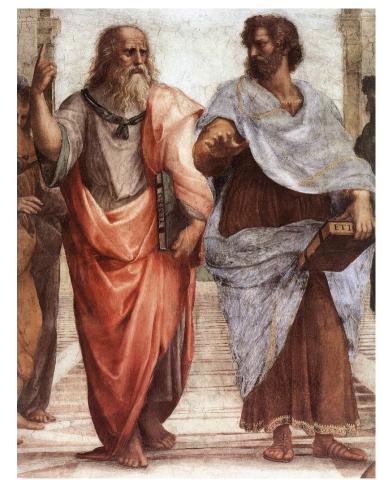
You could do a case study. Choose a set of tasks and use your measurement-based approach to obtain speed as a function of corunners. Now, you have a taskset. Then run your schedulability analysis on this taskset.

OK, I buy that you can obtain these lower bounds on the speed of execution through measurements. But I wonder how trustworthy these numbers are. Have you done any validation?



Then run the measure res of each ta

Then run the system and measure response times of each task. If you observe one case where the observed response time > calculated upper bound on response time, then you have falsified your theory; otherwise, you have corroborated your theory.



5.3 Validation of Model and Schedulability Analysis

We want to compare the computed upper bound on the response time of a task against the measured response times of jobs of this task in order to find out if there is any case in practice where the measured response time of this task exceeds the upper bound on the response time of this task. Even so, the schedulability analysis would be unsafe. To get insight into this question, we pursue a case study with a specific taskset and a real embedded platform (ARM Cortex-A9 quad-core processor). To avoid cache-related preemption delay, we used the software cache partitioning implementation of Linux/RK (Kim et al. 2013)³ and assigned a private cache partition to each task.

We constructed a taskset as follows. First, we created six synthetic programs with different intensities of memory accesses on the target platform. We call each such program a *building block*. There is no shared variable between building blocks. We characterize the execution time and corunner interference using the method in the previous section with SS := 100. The corunner description is complete; that is, the building block is characterized for each possible set of corunners.

Then we create tasks from these building blocks as follows: Task τ_1 consists of executing building block 1. Hence, we model task τ_1 as having a single segment. Task τ_2 consists of executing building block 2 and then executing building block 3. Hence, we model task τ_2 as having two segments. Task τ_2 consists of executing building block 4. Hence, we model task τ_3 as having a single segment. Task τ_4 consists of executing building block 5. Hence, we model task τ_4 as having a single segment. Task τ_5 consists of executing building block 6. Hence, we model task τ_4 as having a single segment. Task τ_6 consists of executing building block 6. Hence, we model task τ_5 as having a single segment. Task τ_6 consists of executing building block 2 and then executing building block 6. Hence, we model task τ_5 as having a single segment. Task τ_6 consists of executing building block 2 and then executing building block 6. Hence, we model task τ_6 as having two segments.

We assign tasks to processors and assign priorities to tasks and assign T and D parameters and obtain the execution time and corunner interference parameters from the building blocks. This gives us the taskset specified in Table 5. The CO-parameters are not shown because they consume lots of space; these parameters are available at the end of the source-code file of the tool that performs schedulability testing.

Our tool yields the following upper bounds on response times of task: 0.113 for τ_1 , 0.554 for τ_2 , 0.132 for τ_3 , 0.153 for τ_4 , 0.146 for τ_5 , and 0.407 for τ_6 (units in seconds).

We run the system for 1,000 seconds and measure the response times of jobs. For task τ_i , we record the maximum response time of a job of this task and let r_i denote it. From the experiment, we obtain $r_i = 0.07$, $r_2 = 0.433$, $r_3 = 0.137$, $r_3 = 0.137$, $r_3 = 0.142$, $r_6 = 0.365$ (units in seconds). With these figures, we obtain that the response time overestimates the observed response times by less than 15%. From this experiment, we see that (1) no deadline was missed and (3) the observed response to the computed upper bound.

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From B. Andersson et al., ``Schedulability Analysis of Tasks with Co-Runner-Dependent Execution Times,'' ACM TECS, 2018:

With these figures, we obtain that the response time overestimates the observed response times by less than 15%. From this experiment, we see that (1) no deadline was missed and (3) the observed response times were close to the computed upper bound.

Conclusion: It is possible to analyze timing of software executing on undocumented multicore.

Thanks!