Towards Sentient Chips: Self-Awareness through On-Chip Sensemaking

Nikil D. Dutt[1]
Center for Embedded and Cyber-Physical Systems (CECS)
University of California, Irvine
dutt@uci.edu
http://www.ics.uci.edu/~dutt
https://duttgroup.ics.uci.edu

[1] **Joint work with Santanu Sarma and Dutt Research Group**

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Towards **Sentient** Chips: Self-Awareness through On-Chip Sensemaking

sen·tient
/ˈsenCH(ē)ənt/

adjective
adjective: **sentient**

able to perceive or feel things.
"she had been instructed from birth in the equality of all sentient life forms"
synonyms: (capable of) feeling, living, live; More

Origin

LATIN LATIN
sentire → sentient- → sentient
feeling *early 17th century*

early 17th century: from Latin *sentient-* 'feeling,' from the verb *sentire* .

Towards Sentient Chips: Self-Awareness through On-Chip

Self-awareness

From Wikipedia, the free encyclopedia

Not to be confused with Self-concept, Self-consciousness, Self-perception, or Self image.

This article has multiple issues. Please help improve [hide] it or discuss these issues on the talk page.

- This article **may require cleanup to meet Wikipedia's quality standards**. *(March 2009)*
- This article **needs attention from an expert on the subject**. *(May 2009)*

Self-awareness is the capacity for introspection and the ability to recognize oneself as an individual separate from the environment and other individuals.

Contents [hide]

1 In philosophy
2 In biology
  2.1 Animals
  2.2 Evolution
  2.3 Neurological basis

The mirror test is a simple measure of self-awareness.

Self-Awareness & Adaptation in Biology

[David Gallo: Underwater astonishments, TED]

Self-Awareness vs Context-Awareness

- **Self-Awareness** [Hinchey2006]: System is aware of its ***self states*** ***and behaviors***
- **Context-Awareness** [Parashar 2005] : System is aware of ***context – i.e., its operational environment***

- ***Self-configuring*** -> capability of reconfiguring automatically
- ***Self-healing*** [Robertson2005] -> *self-diagnosing and self-repairing*
- ***Self-optimizing***-> *capability of self-tuning* or *Self-adjusting*
- ***Self-protecting*** -> capability of detecting dangerous outcomes (e.g. security breaches) and recovering from their effects

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A Hierarchical View

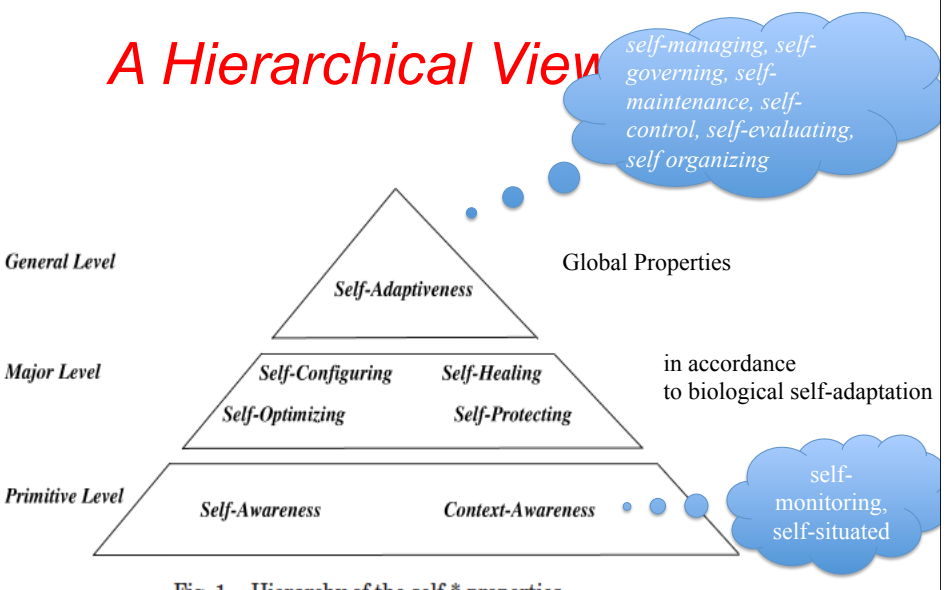

Fig. 1. Hierarchy of the self-* properties.

[SALEHIE 2009, TAAS]

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Self-Reflection

- ***Self-Reflection***:
  - Ability to create a ***self-model***
  - Ability to model their own body/structure (usually known ***self-modeling***)
  - Ability to model their own ***behavior***
  - ***Metacognition capacity****: 'models one's own thinking', 'think about thinking'*
  - *System with* ***two/multiple minds:*** *one* ***being modeled*** *and other* ***doing modeling***
  - ***Control Systems Theory:*** *also called* ***Dynamical System identification***

Towards Sentient Chips: Self-Awareness through On-Chip **Sensemaking**

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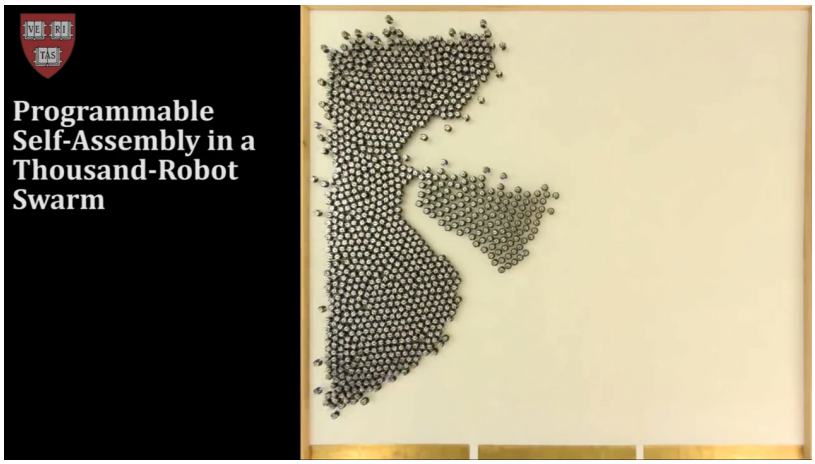
Sensemaking

From Wikipedia, the free encyclopedia

Sensemaking is the process by which people give meaning to experience. While this process has been studied by other disciplines under other names for centuries, the term "sensemaking" has primarily marked three distinct but related research areas since the 1970s: Sensemaking was introduced to Human–computer interaction by PARC researchers Russell, Stefik, Pirolli and Card in 1993, to information science by Brenda Dervin, and organizational studies by Karl Weick.

In information science the term is most often written as "sense-making." In both cases, the concept has been used to bring together insights drawn from philosophy, sociology, and cognitive science (especially social psychology). Sensemaking research is therefore often presented as an interdisciplinary research

Self-Assembling Robots (Sensemaking)



[Kilobots, Harvard 2014]

Outline

- Self-Awareness, Sentience, Sensemaking
- Cyber-Physical Systems-on-Chip (CPSoC)
- CPSoC Exemplars and Prototype
- Wrap-up

Outline

- Self-Awareness, **Sentience**, Sensemaking
- Cyber-Physical Systems-on-Chip (CPSoC)
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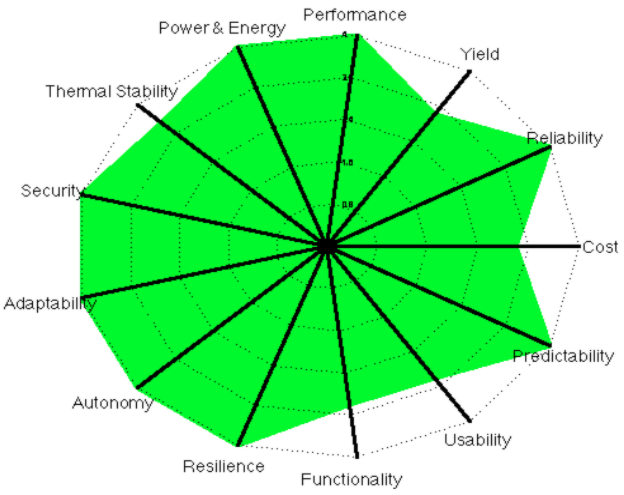
What are Sentient Chips?

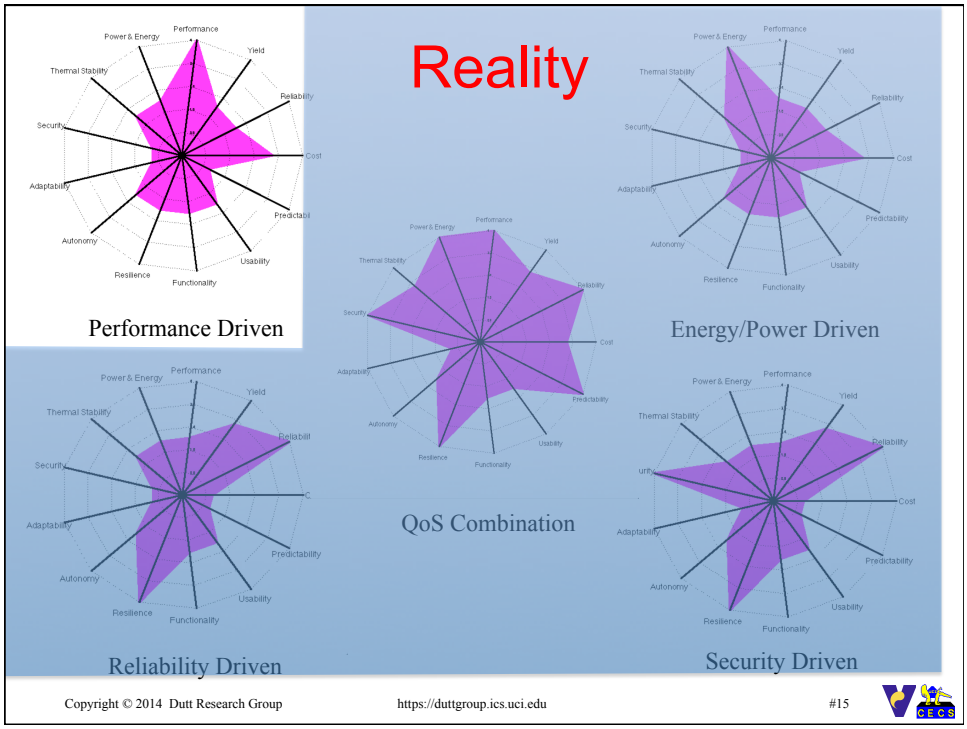
- Sentient chips
  - ***Construct model*** of behaviors and environment using sensor data
  - Achieve ***self-awareness*** through on-chip sensors and monitors
    - Experience phenomena
    - Aware of state and behavior
  - The ability to ***introspect***
  - ***Adapt behavior*** based on model of external and internal environment

Why On-Chip Self-Awareness?

- Tremendous variation in applications, environment, platforms
- Chips must adapt to Dynamic Performance, Power, Resilience, Security,….
  - See Radar chart (Kiviat graph) examples
- Provide Guarantees
- Exploit trade-offs in several dimensions

Ideal Radar Chart?





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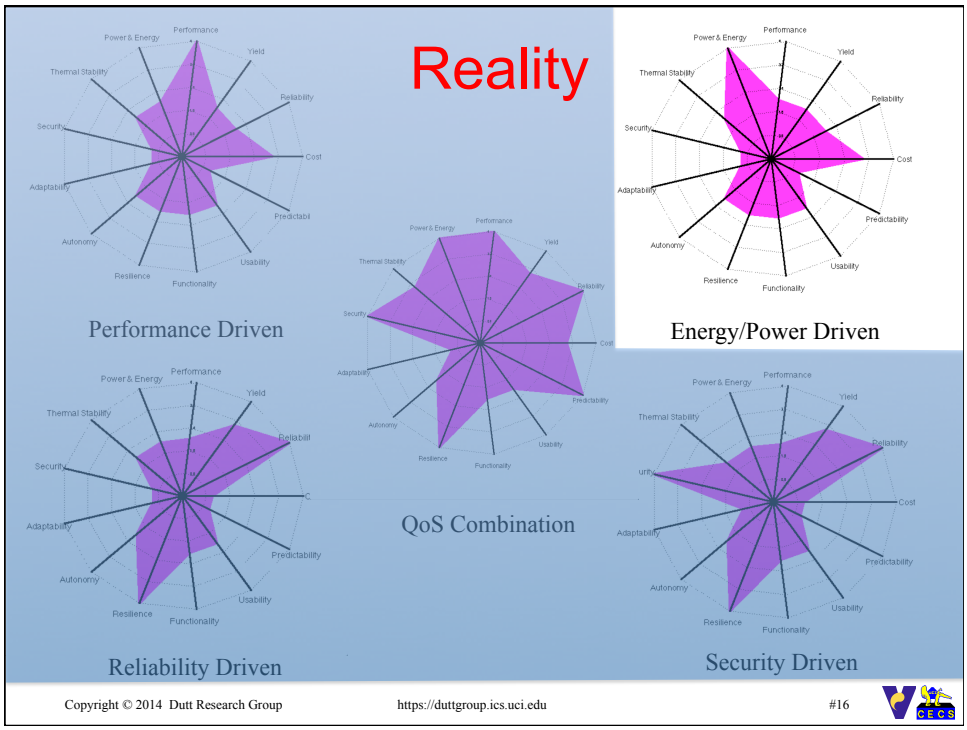

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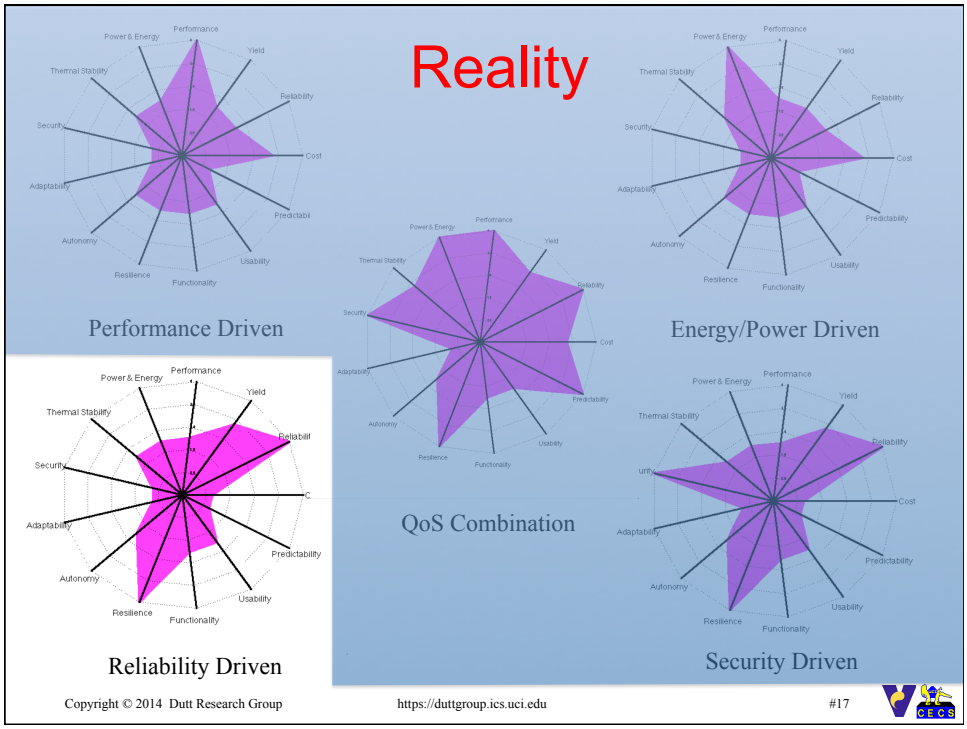
Reality
Performance Driven
Energy/Power Driven
QoS Combination
Reliability Driven
Security Driven
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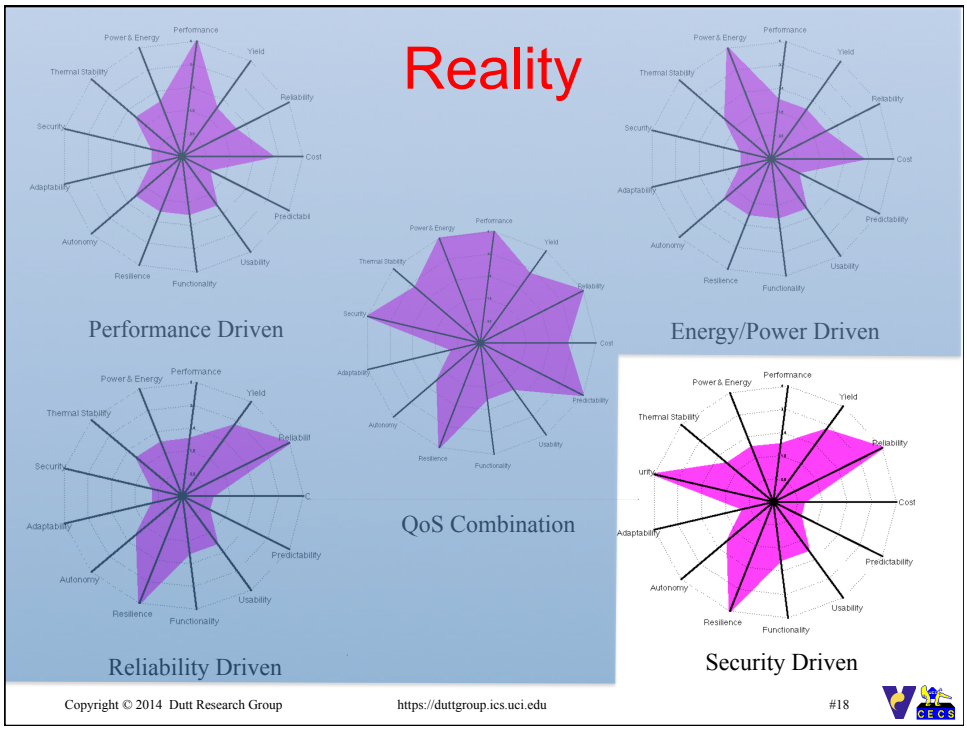
Reality
Performance Driven
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QoS Combination
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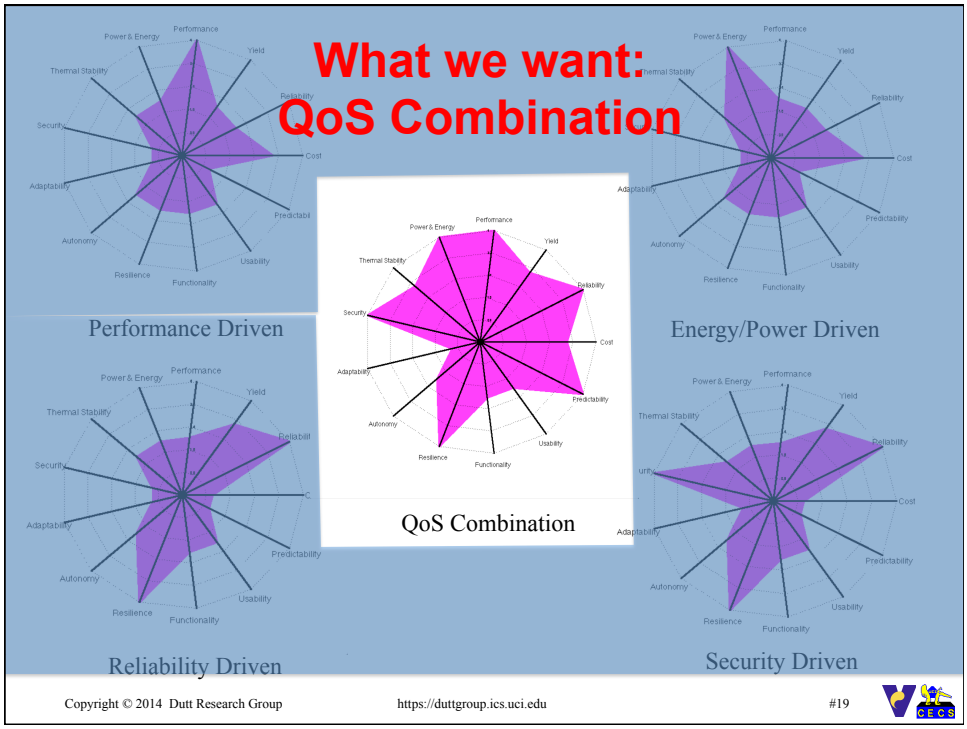
What we want:
QoS Combination
Performance Driven
Energy/Power Driven
QoS Combination
Reliability Driven
Security Driven
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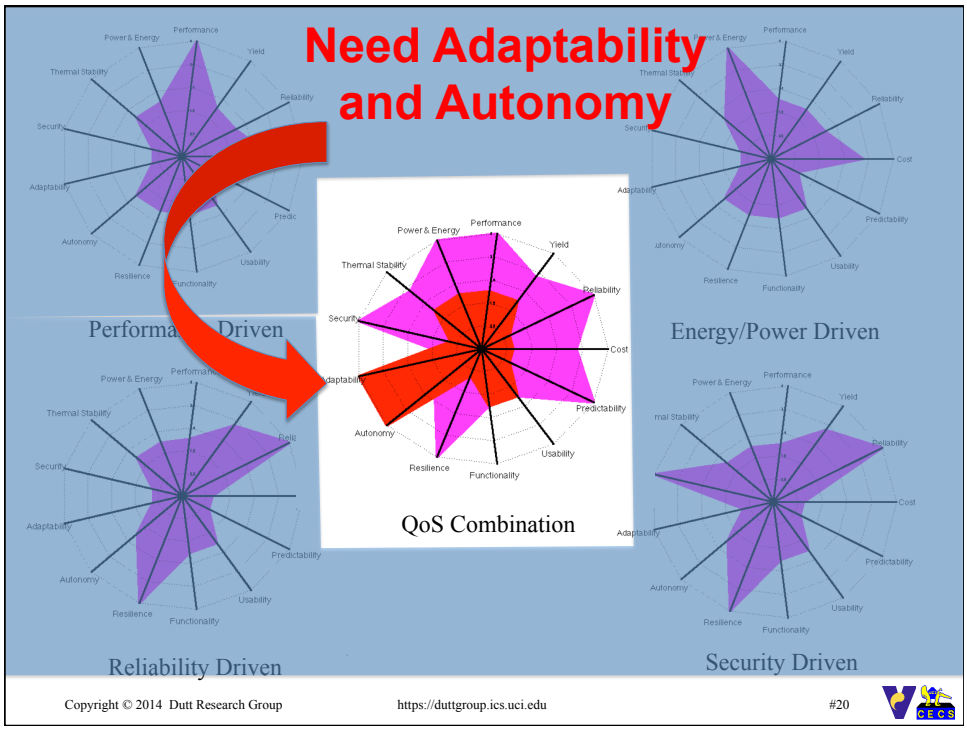
Need Adaptability and Autonomy
Energy/Power Driven
QoS Combination
Reliability Driven
Security Driven
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Outline

- Self-Awareness, Sentience, Sensemaking
- Cyber-Physical Systems-on-Chip (CPSoC)
  - First Step Towards Sentient Chips
- CPSoC Exemplars and Prototype
- Wrap-up

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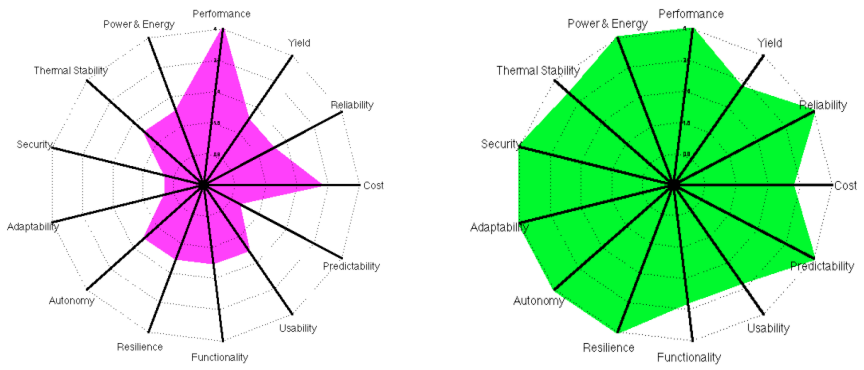
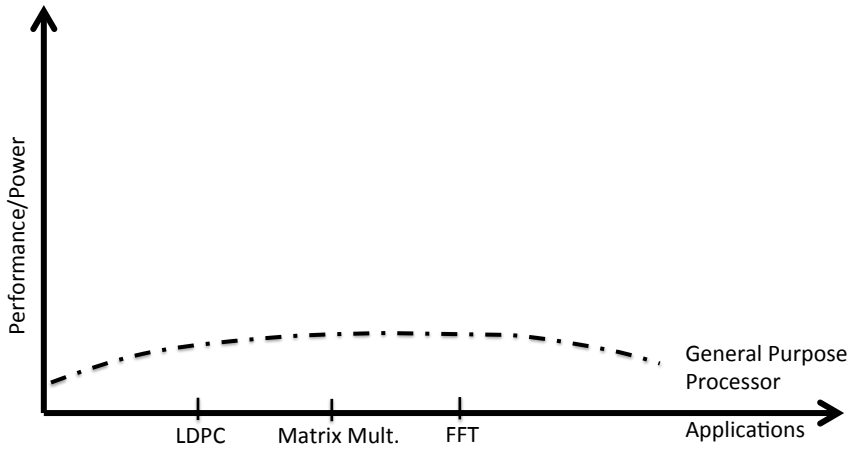
CPSoC Vision: Across Design Features



CPSoC provides opportunity to improve multiple design dimensions (in addition to performance)

CPSoC Vision: Across Applications



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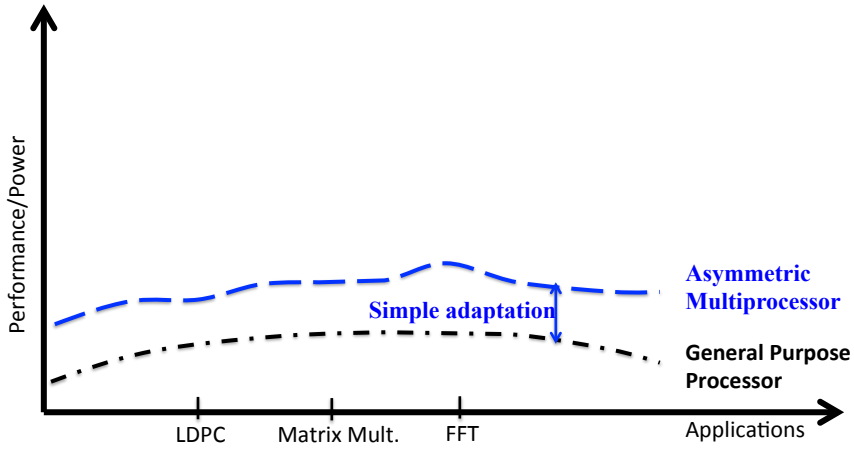
CPSoC Vision: Across Applications



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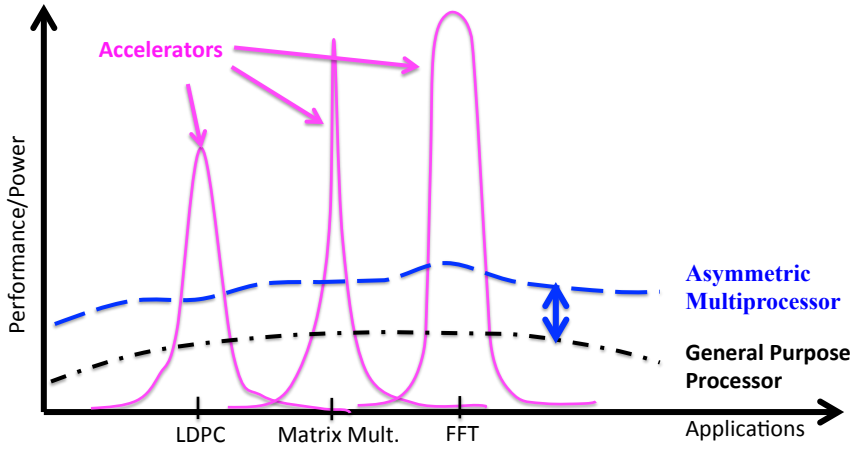
CPSoC Vision: Across Applications



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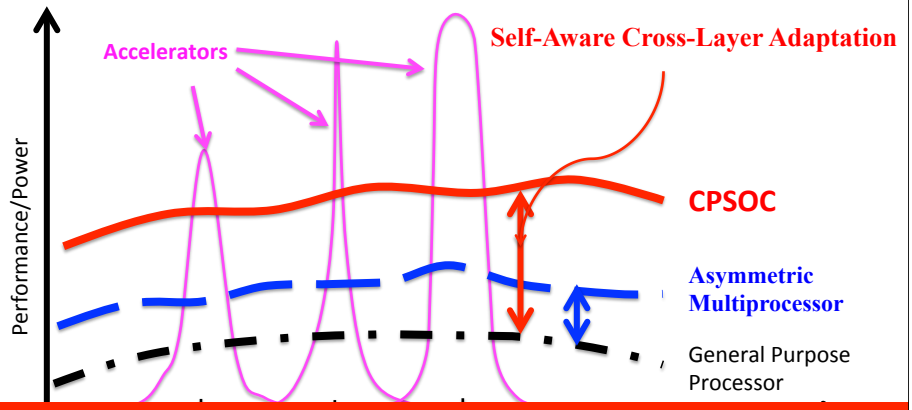
CPSoC Vision: Across Applications



CPSoC aims to adapt across a wide range of dynamic applications to yield acceptable QoS

Cyber-Physical System-on-Chip (CPSoC)

- ***Cross-Layer Virtual and Physical Sensing & Actuation***
  - **Sensor fusion and Actuation**
    - Combine hardware and software sensors
- ***Self-Awareness and Adaptation***
  - Combines ***Simple*** and ***Self-Aware*** adaptions
  - A reflexive (**Observe-Decide-Adapt**) architecture to achieve closed loop system control
- ***Predictive Modeling & Learning***
  - Dynamic characterization of platform variability across multiple levels of the system stack.

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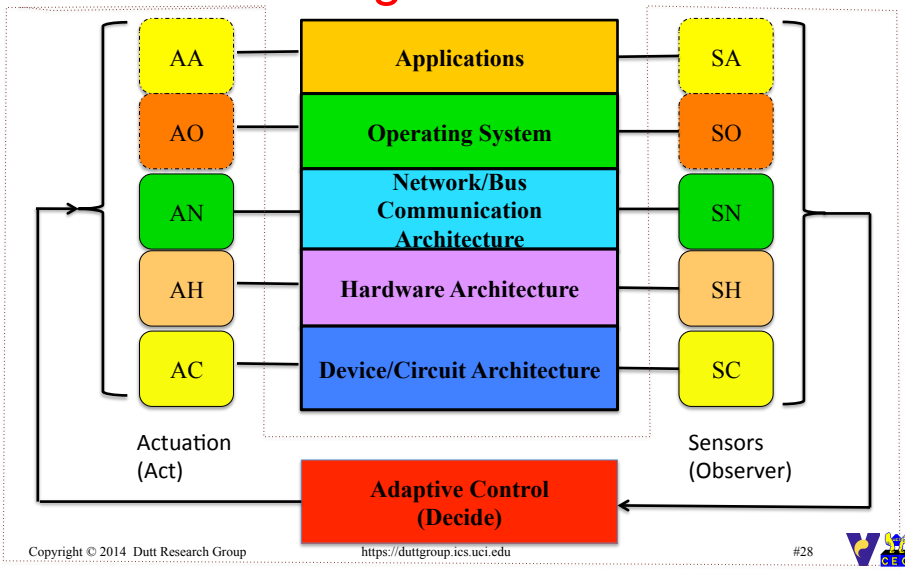
Cross-Layer Physical/Virtual Sensing & Actuation



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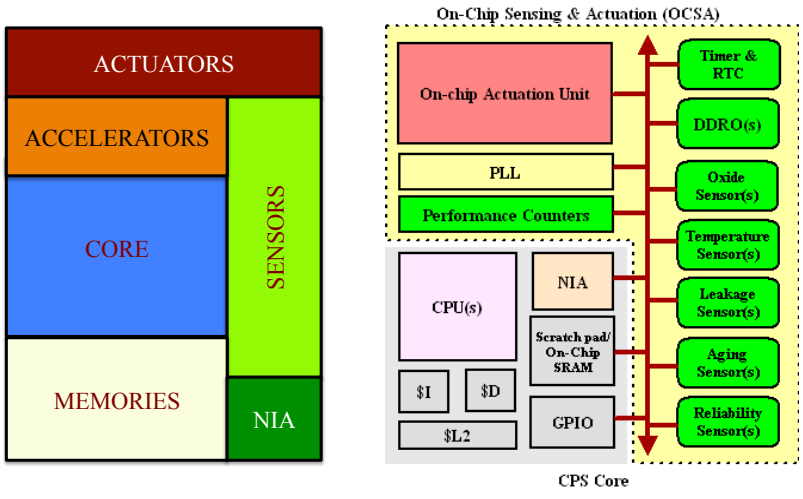
Examples of Virtual Sensors and Actuators Across Layers of CPSoC

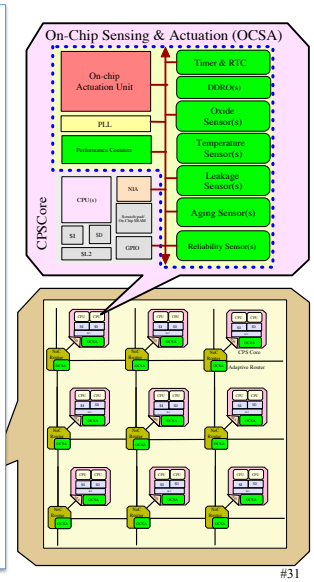
Layers	Virtual/Physical Sensors	Virtual/Physical Actuators
Application	Execution Time, Workload Power, Energy,	Loop perforation Algorithmic Choice
Operating System	System Utilization Peripheral States	Task Allocation, Scheduling, Migration, Duty Cycling
Network/Bus Communication	Bandwidth; Packet/Flit status; Channel Status, Congestion, Latency	Adaptive Routing Dynamic Bandwidth Allocation Ch. no and direction
Hardware Architecture	Cache misses, Miss rate; access rate; IPC, Throughput, ILP/MLP, Core asymmetry	Cache Sizing; Reconfiguration, Resource Provision Static/Dynamic Redundancy
Circuit/Device	Circuit Delay, Aging, leakage Temperature, oxide breakdown	DVFS, DFS, DVS ABB, Clock and Power-gating

CPSoC Basic Computational Block

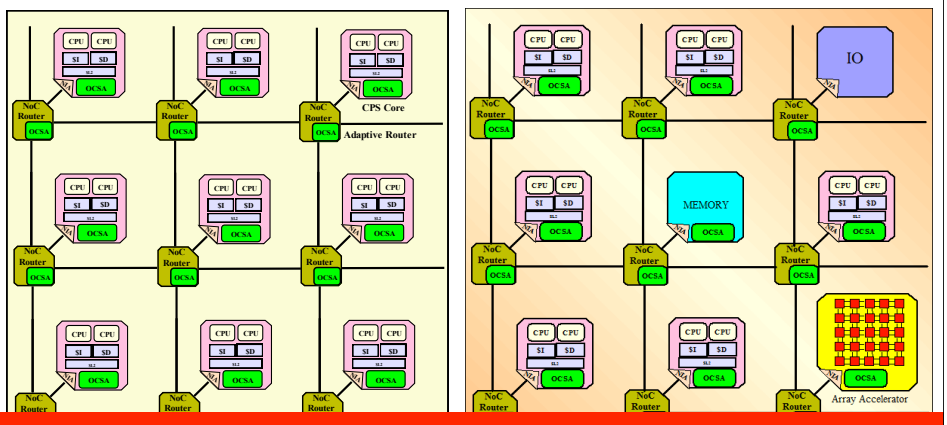


CPSoC Computational Platform

- Sensor/Actuator-rich SoC fabric
  - **OCSA: On-Chip Sensing and Actuation unit**
- NoC overlay (or separate network)
- SW enabled sensors & actuators
- Adaptive control of platform resources

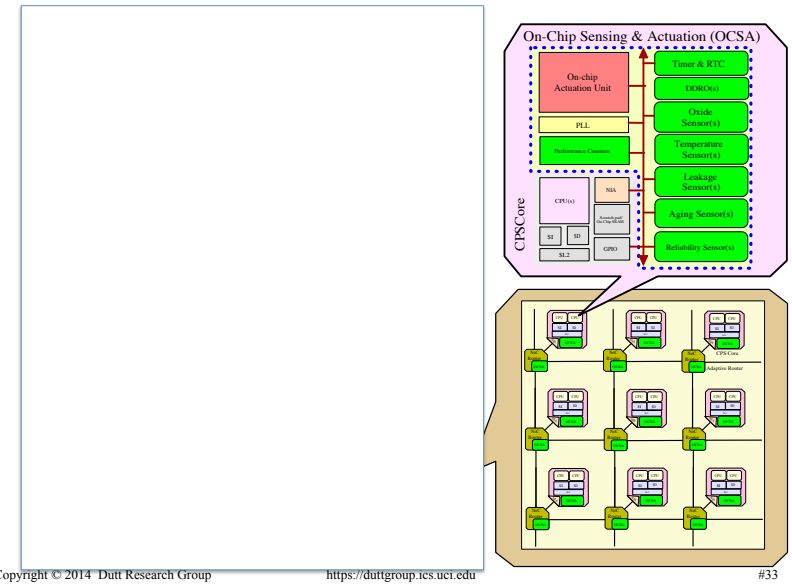


CPSoC Hardware Fabric

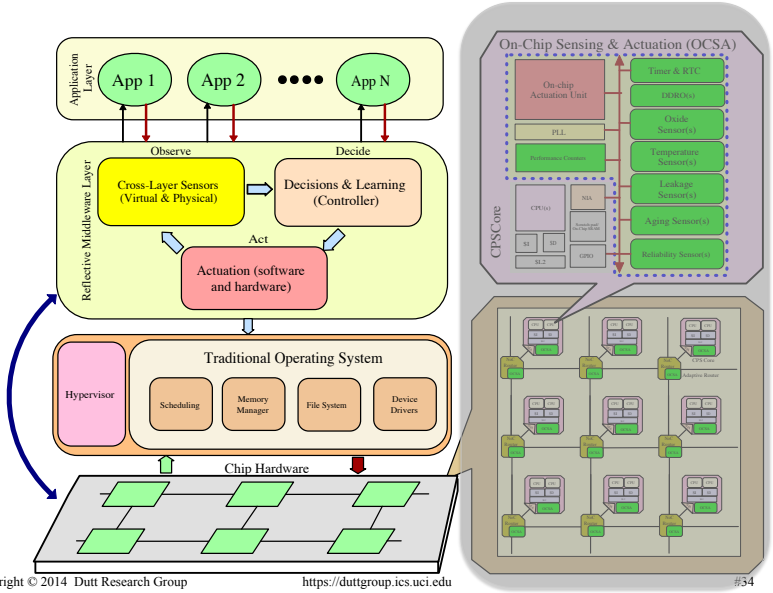


Distributed resources supporting homogeneous or heterogeneous or mixed fabric

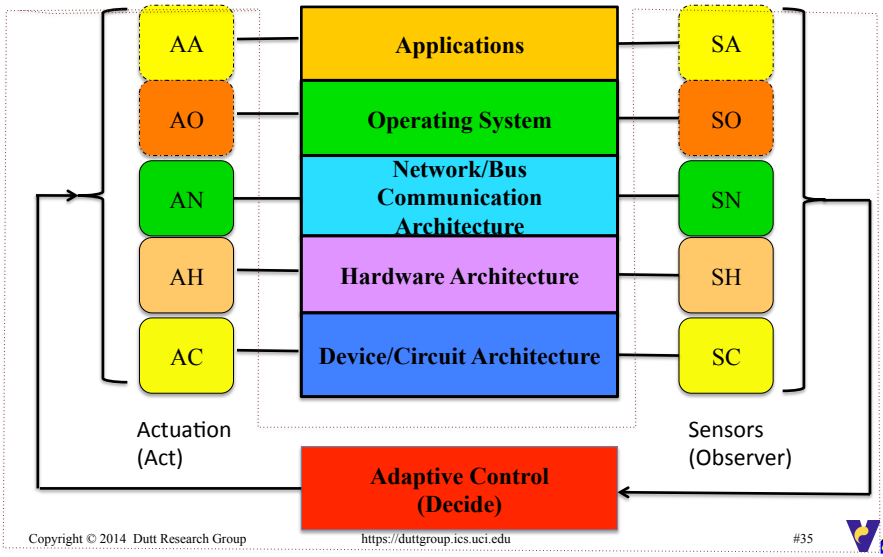
CPSoC HW/SW Stack



CPSoC HW/SW Stack



Cross-Layer Physical/Virtual Sensing & Actuation



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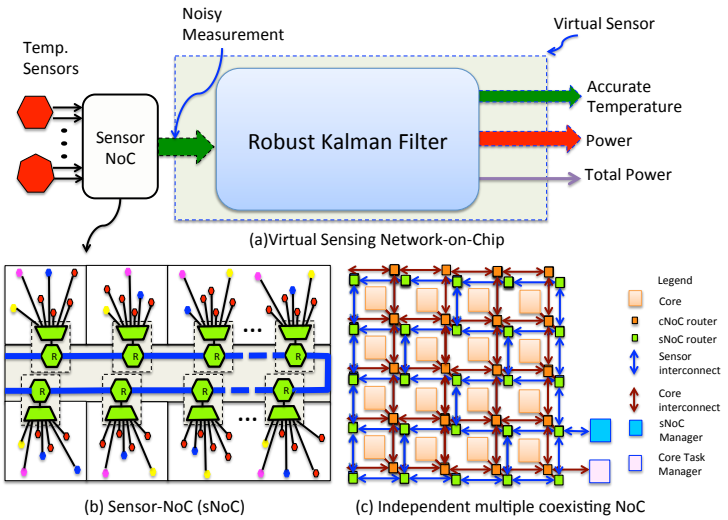
Cross-Layer Physical/Virtual Sensing

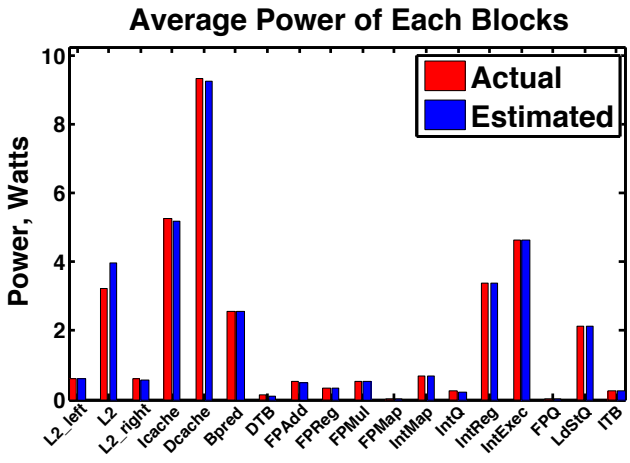
- Many restrictions in physical deployment of sensors and test structures in MPSoCs:
  - Resource constraints
    - e.g., Area, Power
  - Limited number, resolution, accuracy, range
  - Placement Restrictions
  - Complexity of sensing and observation structures
  - Inaccessibility or inability of direct measurement
  - Prohibitive cost

Virtual Sensing is a Indirect Computational Approach to overcome several sensing limitations

Example Virtual Power Sensing with few Thermal Sensors



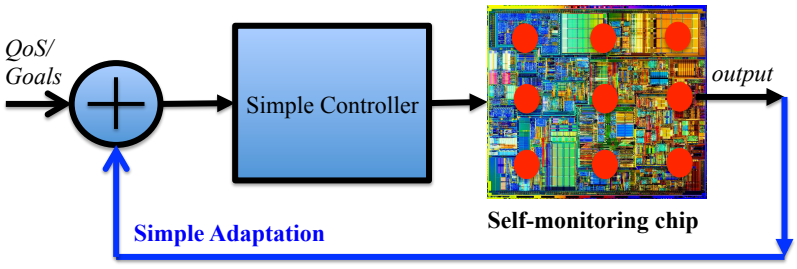
Example Virtual Power Sensing with few Thermal Sensors



Cyber-Physical System-on-Chip (CPSoC)

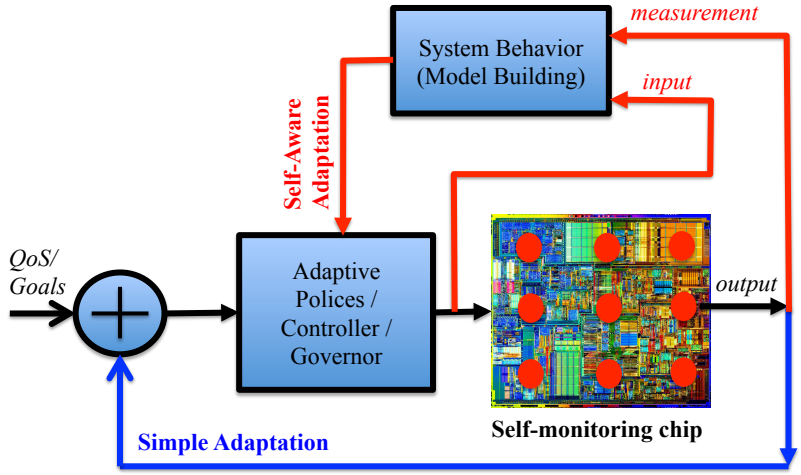
- *Cross-Layer Virtual and Physical Sensing & Actuation*
  - Sensor fusion and Actuation
    - Combine hardware and software sensors
- ***Self-Awareness and Adaptation***
  - Combines ***Simple*** and ***Self-Aware*** adaptions
  - A reflexive (**Observe-Decide-Adapt**) architecture to achieve closed loop system control
- ***Predictive Modeling & Learning***
  - Dynamic characterization of platform variability across multiple levels of the system stack.

MPSoC with Simple Adaptation



Self-monitoring and **simple adaptation**

Sentient Chips (Self-Awareness): CPSoC



Self-monitoring and **behavior modeling** [Sarma14, CODES+ISSS14]

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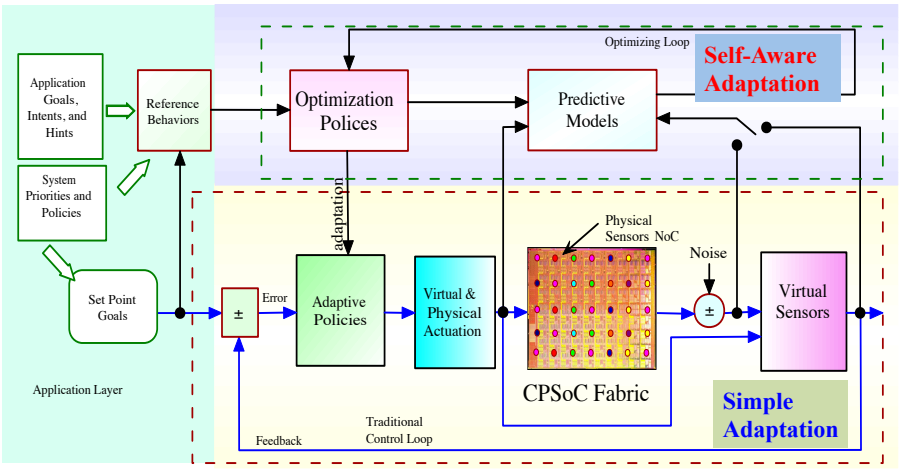
CPSoC Context



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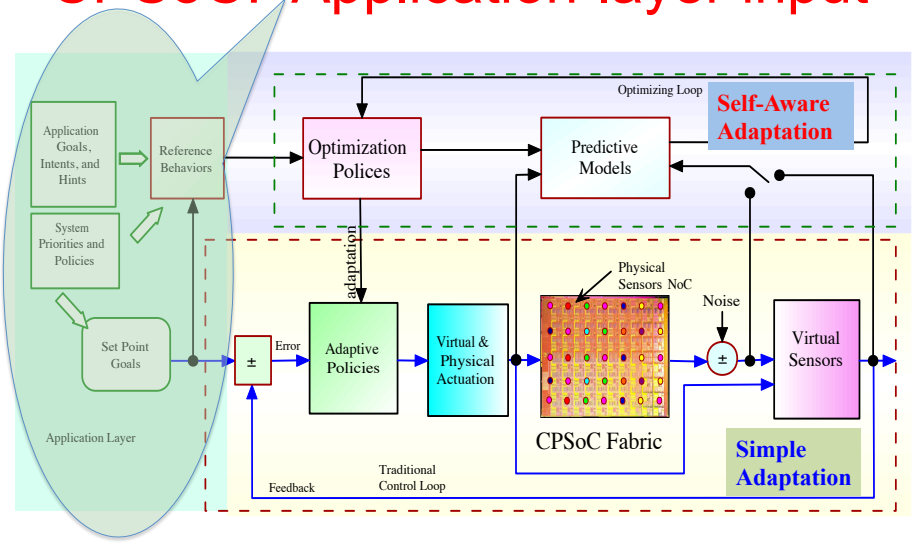
CPSoC: Application-layer input



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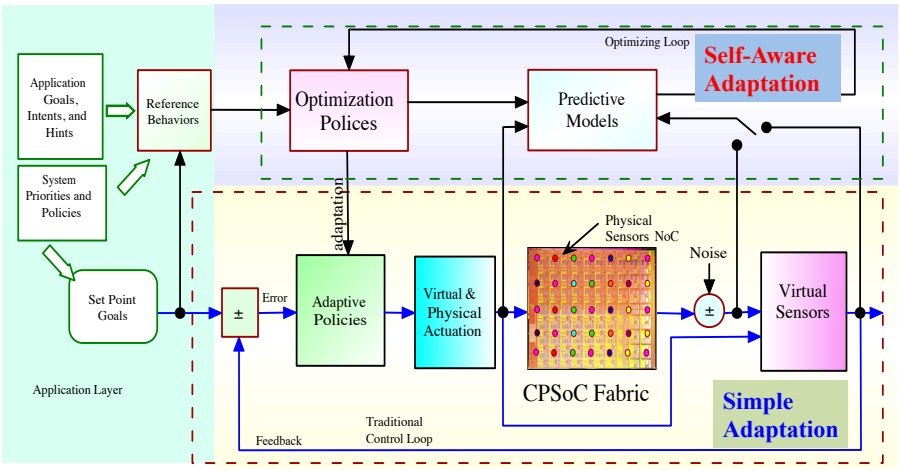
CPSoC: Two Adaptation Loops



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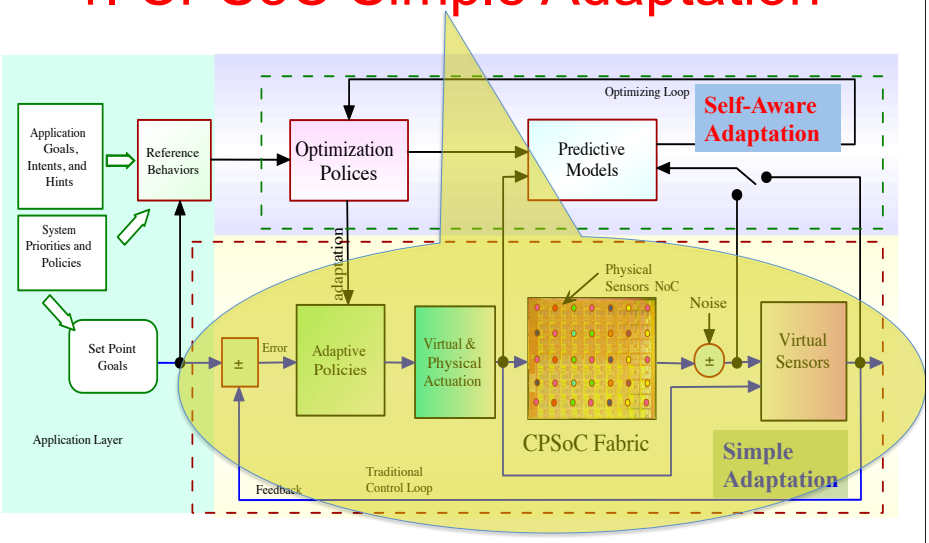
1. CPSoC Simple Adaptation



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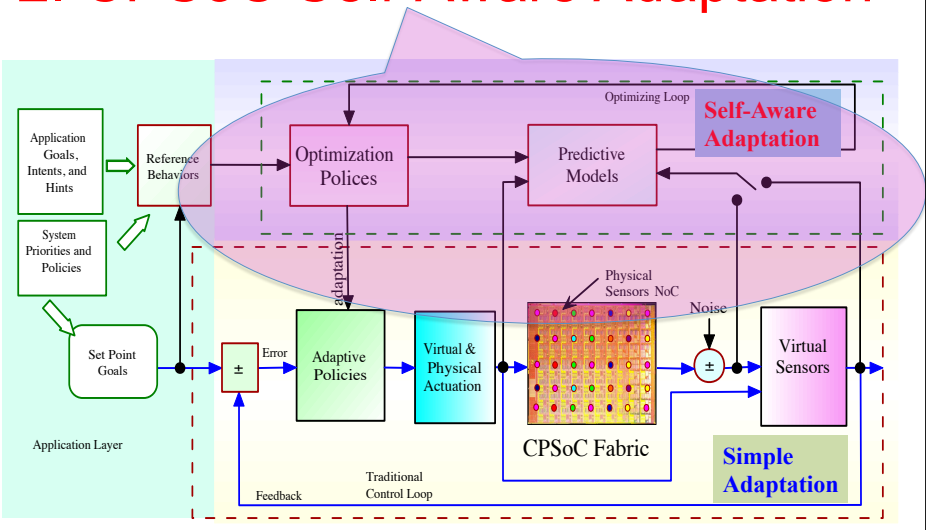
2. CPSoC Self-Aware Adaptation



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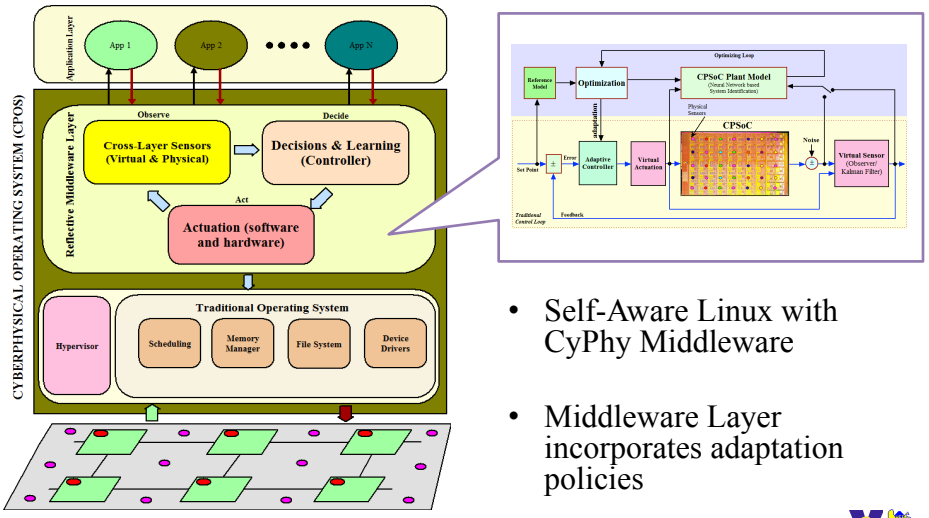
Adaptive, Reflexive CyPhy Middleware



- Self-Aware Linux with CyPhy Middleware
- Middleware Layer incorporates adaptation policies

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Outline

- Self-Awareness, Sentience, Sensemaking
- Cyber-Physical Systems-on-Chip (CPSoC)
- CPSoC Exemplars and Prototype
- Wrap-up

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Sample Application and Use cases

- Energy Efficiency (Throughput/Power)
  - Dynamic Workloads
  - Opportunistic Load balancing
  - Adaptive Scheduler
  - Evolutionary Approach
- Thermal-Aware Performance
  - Dynamic/Adaptive Parallelization
  - Heterogeneous Architecture
  - Adaptive Scheduling
- Aging and Resilience
  - Opportunistic Allocation
  - Duty cycling of Active and Resting periods

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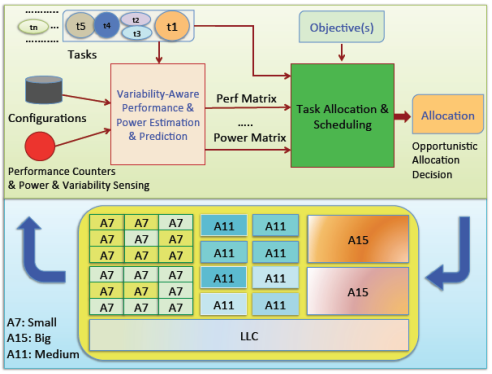
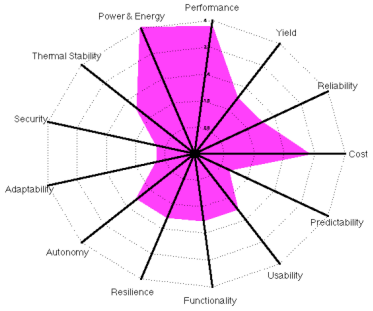
Energy Efficiency Improvement





Goal:
- **Energy Efficiency**

[Sarma13, CECS TR]

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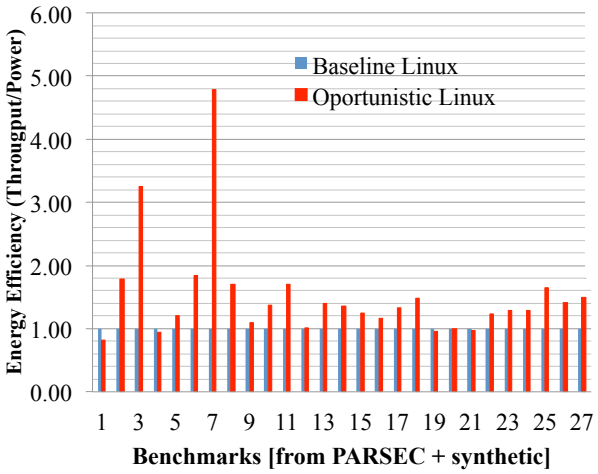
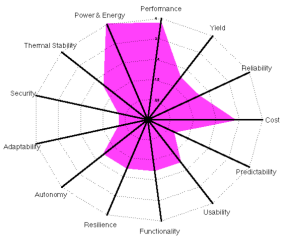
Energy Efficiency Improvement

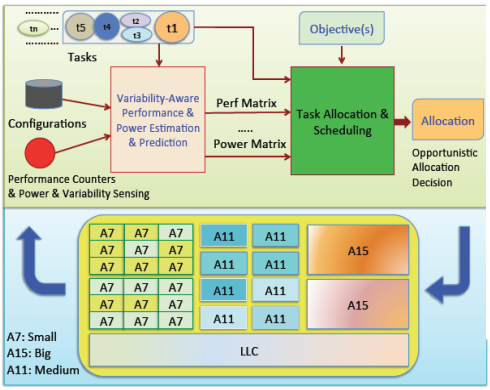


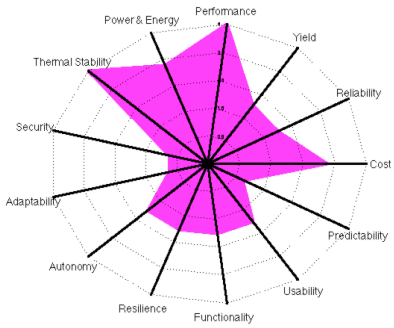


51% Average Improvement for Quad-core

[Sarma13, CECS TR]

Thermal-Aware Performance

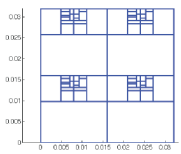




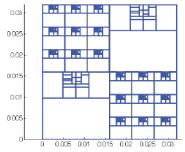
Goal:

- **Improve throughput under max temp & power constraint**

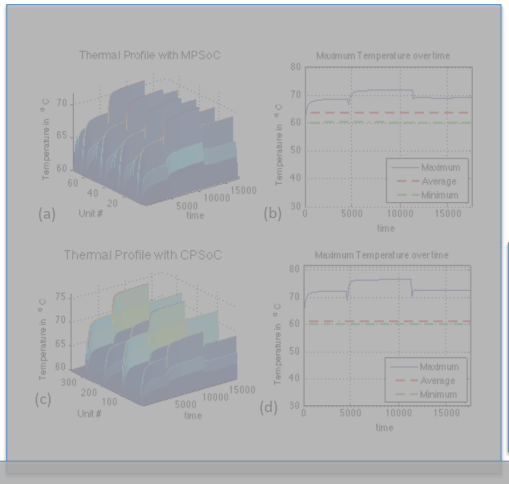
Thermal-Aware Performance



4 core



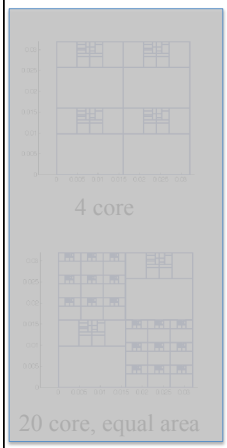
20 core, equal area

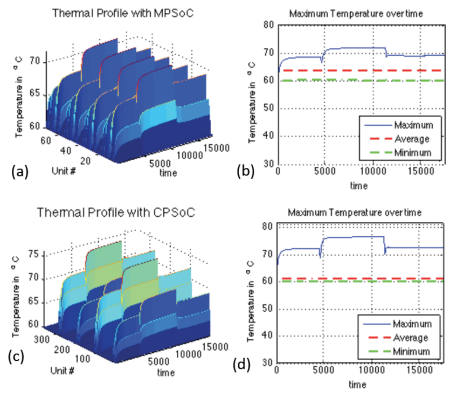


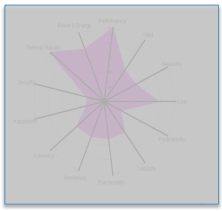
Throughput Improved by 70% -300% For same power & peak temp

For same power consumption and peak temperature, throughput improved

Thermal-Aware Performance



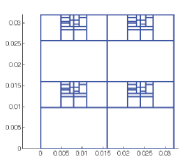




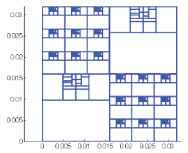
Throughput Improved by 70% -300% For same power & peak temp

Throughput improved for same power and peak temperature!

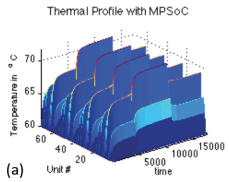
Thermal-Aware Performance

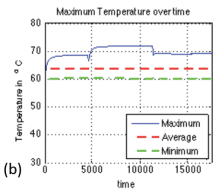


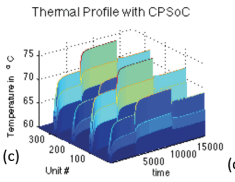
4 core

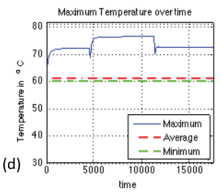


20 core, equal area









Throughput Improved by 70% -300% For same power & peak temp

For same power consumption and peak temperature, throughput improved

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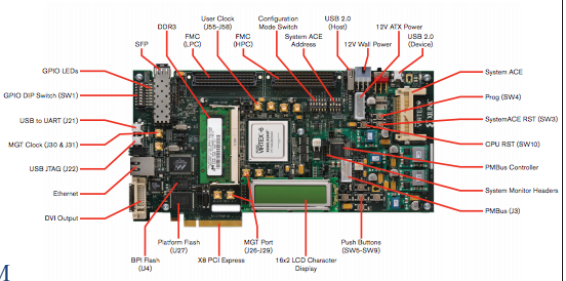
CPSoC FPGA Prototype

- Goal: validate simulation studies for task migration, temperature, wear-out, etc.
- Platforms: Virtex 5 and Virtex 6
- Processor Core : SPARC/Leon 3, Leon 2, S1
- No Of Processor : 2-8
- NoC : Mesh Connected, 200-800 MBPS Bandwidth
- On-chip Memory : 16-64kB per core
- External Memory: 4 GB of DRAM
- Sensors:
  - Ring Oscillators: 20-50
  - Thermal: 20-40
  - Aging: 10-20
  - Razor/EDS: 20-50
- OS: Linux 2.x/3.x

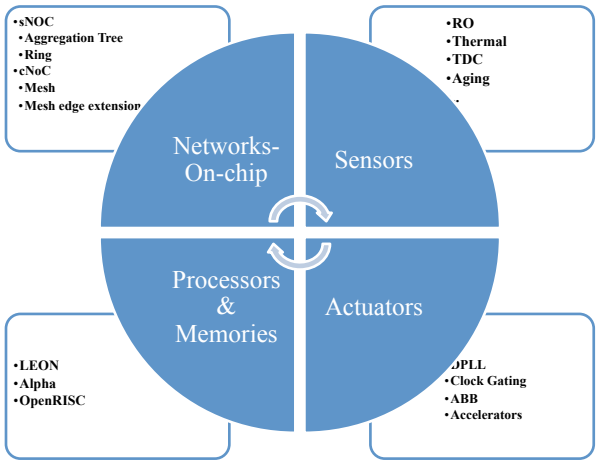


Xilinx Vertex 6 Board

[Sarma14, RSP14]

NSF Expedition in Computing, Variability-Aware Software for Efficient Computing with Nanoscale Devices http://variability.org

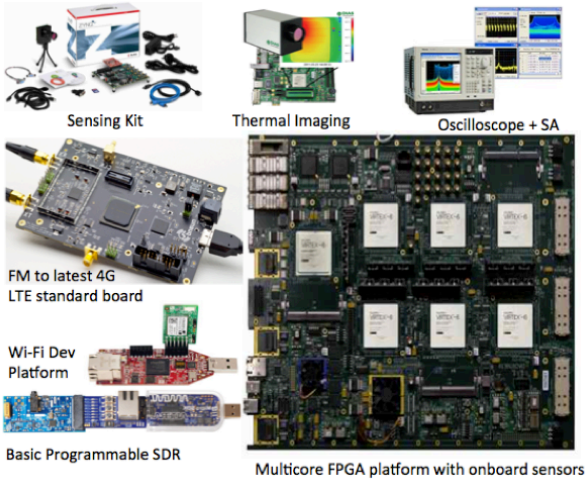
FPGA Library for CPSoC



Develop an FPGA library to construct CPSoC

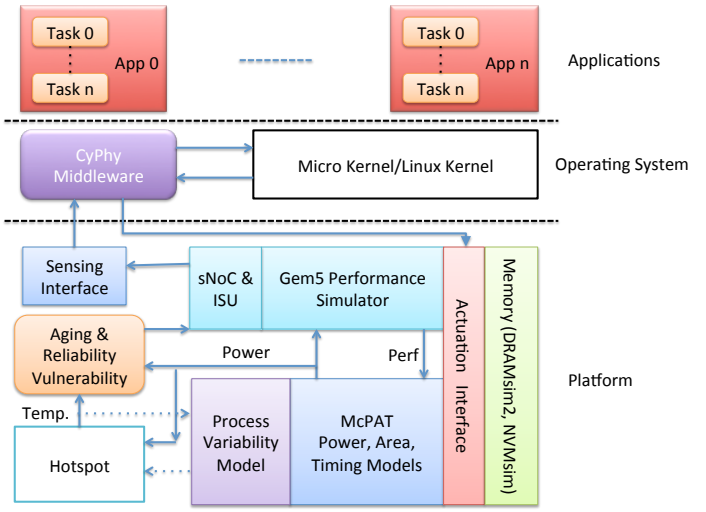
[Sarma14, RSP14]

CPSoC Multi-FPGA Distributed Platform



[Sarma13, CECS TR]

CPSoC Simulation Framework

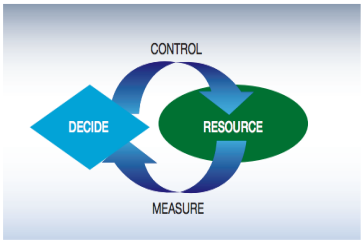


[Sarma14, RSP14]

Self-* Computing: Related Efforts

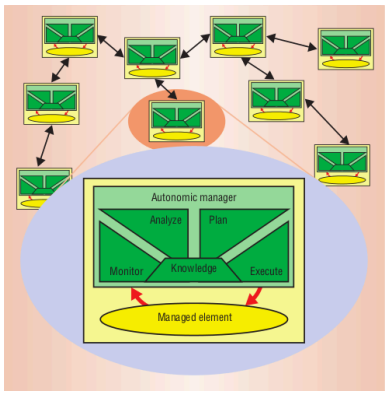
- Autonomic Computing (IBM)
- SEEC (MIT & Milano)
  - Software centric/focused adaptation with homogeneous arch
  - Uses ODA loop for feedback control
- Invasive Computing (Erlangen & KIT)
  - Adaptive use of computing platform resources
  - Distributed management
  - No Self-modeling and system behavior identification

Self-Awareness in Software Systems (IBM's Autonomic Computing)



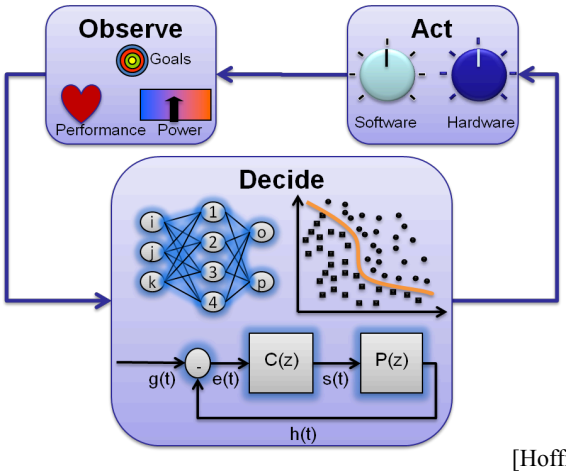
From *Autonomic Computing Concepts*, IBM White Paper, 2001

[Kephart2003]



[Autonomic Computing, IBM]

SEEC [MIT+Milano]

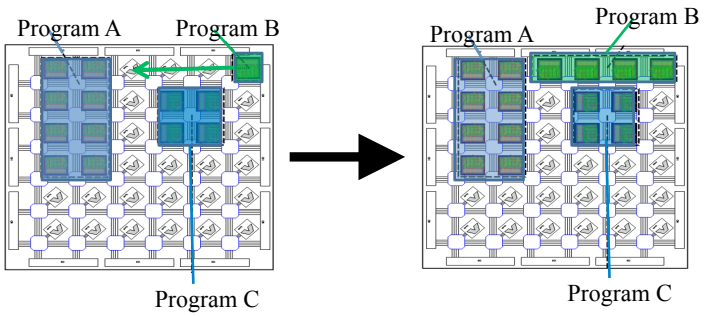


[Hoffmann2012, DAC]

ODA loop in the self-aware computing model

Invasive Computing (Erlangen/KIT)

- **Definition: Invasive Programming** denotes the capability of a program running on a parallel computer to request and temporarily claim processor, communication and memory resources and to be capable to subsequently free these resources again.



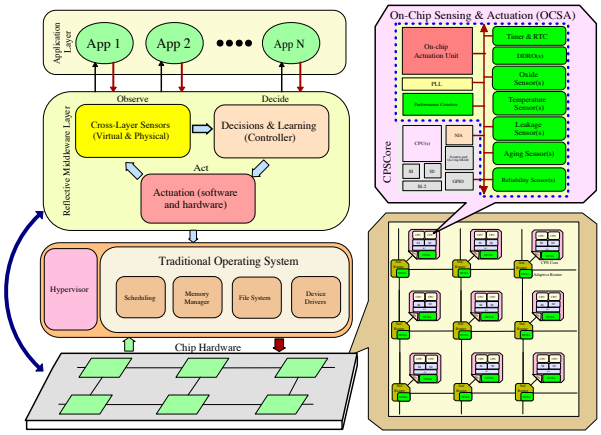
[Kobe11] [www.invasic.de/]

Outline

- Self-Awareness, Sentience, Sensemaking
- Cyber-Physical Systems-on-Chip (CPSoC)
- CPSoC Exemplars and Prototype
- Wrap-up

Key Take-Aways

CPSoC: First step towards Sentient Chips



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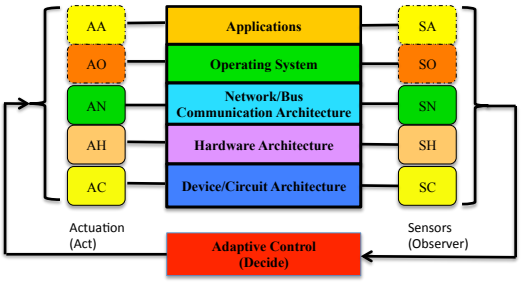
Key Take-Aways

CPSoC: First step towards Sentient Chips

Key CPSoC features:

- ***Cross-Layer Virtual and Physical Sensing & Actuation***
  - Combine hardware and software sensors across multiple layers

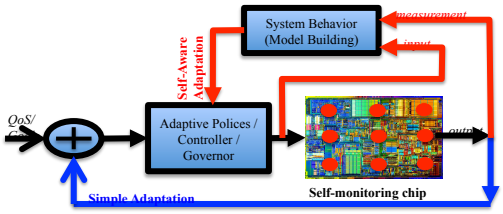


 https://duttgroup.ics.uci.edu #66

Key Take-Aways

CPSoC: First step towards Sentient Chips

Key CPSoC features:



- ***Self-Awareness and Adaptation***
  - ***Simple*** and ***Self-Aware*** adaptions
  - Adaptive, reflexive architecture (*Observe-Decide-Adapt*)
- ***Predictive Modeling & Learning***
  - Dynamic platform characterization across multiple levels

Key Take-Aways

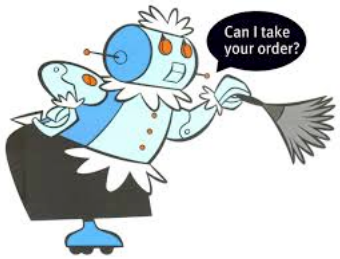
CPSoC: First step towards Sentient Chips

Key CPSoC features:

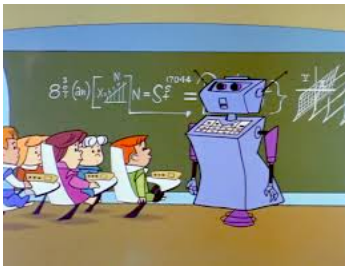
- ***Cross-Layer Virtual and Physical Sensing & Actuation***
  - Combine hardware and software sensors
- ***Self-Awareness and Adaptation***
  - ***Simple*** and ***Self-Aware*** adaptions
  - Adaptive, reflexive architecture (*Observe-Decide-Adapt*)
- ***Predictive Modeling & Learning***
  - Dynamic platform characterization across multiple abstraction levels

Quo Vadis, Sentient Chips?

Good? ***or*** **Evil?**



Professor's Worst Nightmare: MOOCs + Sentient Robots



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  - Lead PhD student on CPSoC theme
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  - Tiago Mück, Majid Shoustari, Bryan Donyanavard, Hossein Tajik, Abbas BanaiyanMofrad, Roger Hsieh, Jurngyu Park
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  - UCLA: Prof. Puneet Gupta
- NSF Variability Expedition Project Team
  - www.variability.org

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Dutt Research Group: http://duttgroup.ics.uci.edu/

NSF Variability Expedition **www.variability.org**

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