SCProcessor Builder: A tool to create and simulate processors in SystemC

Julio Melo, Luiz C. Leite
Federal University of Rio Grande do Norte
Programa de Pós Grad. em Eng. Elétrica e Computação
Natal, Brazil
julio.engcom@gmail.com, leduardocl@gmail.com

Max M. Silveira, Rivaldo Junior, Marcio Kreutz
Federal University of Rio Grande do Norte
Programa de Pós Grad. em Sistemas e Computação
Natal, Brazil
asmiller007@gmail.com, rivaldojr@gmail.com, kreutz@dimap.ufrn.br

Abstract—This paper presents the SCProcessor Builder that consists on a toolset that enables the modeling and simulation of different processor architecture and behavior. The models are designed using XML language and state machines for the structural and behavior parts respectively. The proposed tool converts the models to SystemC in order to simulate the execution of programs on modeled processors.

I. INTRODUCTION

The problem of describing a processor is well known in the digital systems modeling area. This have many components, but most of the times they will be compound of selectors, registers and arithmetic logic units (ALU)[1]. The tool generates a processor using a SystemC[4] compatible with Transaction Level Modeling (TLM)[7].

II. SCPROCESSOR BUILDER

The key concept related with the processor simulation area is the term Architecture Definition Language (ADL). There are several ADLs such as nML[2], Language for Instruction Set Architecture LISA[3] and ARCH-C[5]. The SCProcessor Builder provides a set of tools more focused on processor architecture and control unit modeling. The system enables the definition of each individual structural component of the processor architecture through XML documents and generated SystemC code.

Figure 1. System Developed.

III. RESULTS

Three custom processors were implemented to test the main functionalities of the system. The first one had a simple architecture with a custom instruction set. The second model consisted in an adaptation of the ARM/DLX[6] processor. The last one is a more complex version of the second, consisting on a pipelined version of the ARM/DLX. To test the code execution we built a test bench that includes the generated processor and a testing executable that loads in the processor memory test code.

IV. FINAL STATEMENTS

This work had as main objective the development of a processor design tool able to simulate a processor functionalities and structures in SystemC. The result was a tool set called SCProcessor Builder, that are able to specify and simulate processor architectures based on structural and behavior models provided.

V. REFERENCES